Semiconductor Optoelectronics
ISSN: 1001-5868

DESIGN AND ANALYSIS OF 32-BIT REVERSIBLE ALU FOR LOW POWER APPLICATIONS

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Abstract—All processors use an Arithmetic Logic Unit (ALU) for operations in logic and mathematics. It is a crucial component of the design of digital systems as well. ALUs, which are found in numerous devices equivalent to computers, smart phones, and calculators, are among the most crucial parts of any system. With logical gates for each one-bit ALU circuit, similar to AND and OR,Verilog HDL was used to develop a 32-bit ALU. Xilinx is used to carry out the design. It uses less power and can operate more quickly than an ALU processor. Reversible logic has been increasingly important in recent years because a critical criterion in low power design, because its capacity to lower power dissipation.More power is used by ALUs created using non-reversible logic gates. Reversible logic has been essential in recent years for low power VLSI Design methodologies as a result of the demand for lower power consumption. This method aids in decreasing power consumption and power loss. This study compares a reversible logic gate-based ALU architecture, such as the Peres gate, Feynman gate, Toffoli gate, and Fredkin gate, as opposed to one that uses ordinary logic gates. ModelSim is used to simulate each module, while Xilinx ISE 14.7 is used to synthesise each module.
Index Terms—ALU, Peres gate, Feynman gate, Fredkin gate,Toffoli gate and RI gate

I. INTRODUCTION

More power is used by ALUs created employing logic gates that cannot be reversed. Reduced power consumption is there- fore necessary. Because it can decreased power consumption, a crucial criteria In the Low Power Design VLSI, reversible logic has become increasingly

important in recent years. ALUs now in use use reversible logic gates, such as AND, OR, and NOT.Although they are simple to construct, they have some significant downsides, including increased complexity, pricey circuits, delayed operation, and inefficient power use. Reversible logic gates are thus used in this architecture. Future technologies like photonic computing, ultra-low power Very Large Scale Integration architecture etc. all make considerable use of reversible logic. Due to the fact that reversible circuits have No information or energy is lost, reversible logic is being researched for use in VLSI circuits with minimal power.. Reversible logic design will therefore undoubtedly be im- portant in the future. In this study, a 32-bit reversible arith- metic and logical unit's logical architecture is described and evaluates its efficiency, size, and power in comparison to an irreversible arithmetic and logical unit.

II. REVERSIBLE LOGIC GATES

The n × n logic circuits that make up reversible logic gates in which there is always a 1:1 mapping between the quantity of inputs and outputs.This makes sure that the only way to redeem input is through the outputs. Quantum costs, garbage outputs, constant inputs, and gate count are the factors that determine how well a reversible circuit performs.

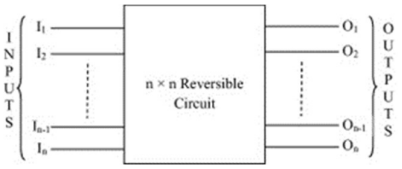


Fig. 1. Reversible Logic Gate

The following is a quick description of the reversible gates utilised in 32-Bit ALU architectures.

A. Peres Gate

Figure 1 shows it a 3 x 3 reversible gate. Here, we employed the Peres gate to achieve the ALU's low quantum cost of 4. Below figure 1 Shows,the inputs and outputs.

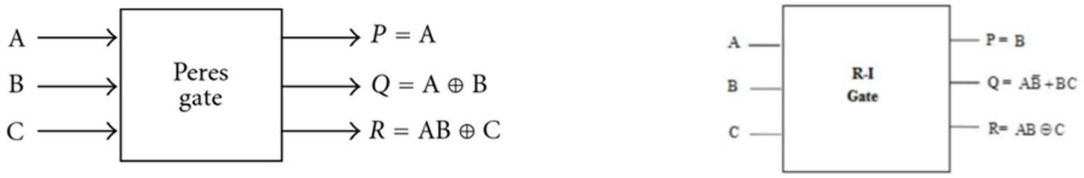
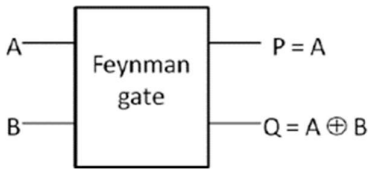


Fig. 2. Peres Gate

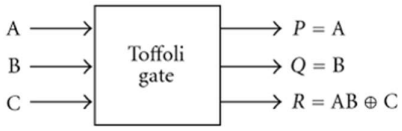
B. Feynman Gate

Quantum cost of 1 is associated with the Feynman gate is sometimes referred to a NOT logic gate. The following figure 2 lists the inputs and outputs.

Fig. 6. RI Gate



III. 32-BIT REVERSIBLE ALU



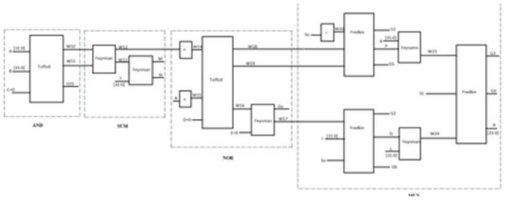


Fig. 3. Feynman Gate

C. Toffoli Gate

A 3 x 3 gate that can be reversed. The below figure 3 lists the inputs and outputs. The alternate term pertaining to this gate, that has a 5 quantum cost, is the ”Doubly controlled NOT gate.”

The block diagram a 32-Bit ALU Reversible is displayed in the image below. The ALU must primarily perform the operations AND, XOR, NOR, and SUM. Every action requires a unique circuit design, which is coupled to achieve the lowest possible lines and gate costs. A 4:1 reversible multiplexer is utilised to obtain the output in a single line. The multiplexer employs Fredkin gates. The ALU is termed AXONS ALU by using a letter from each of the operations it performs, which are AND, XOR, NOR, and SUM. It features two selection lines.

D. Fredkin Gate

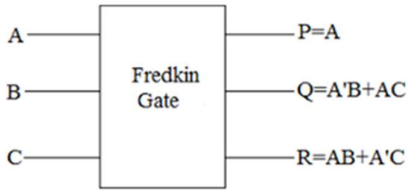


Fig. 4. Toffoli Gate

Fig. 7. 32-BIT REVERSIBLE ALU BLOCK DAIGRAM

It is a reversible 3 x 3 gate. Below Figure 4 shows the inputs and outputs. Quantum cost is 5.

IV. METHODOLOGY

E. RI Gate

Fig. 5. Fredkin Gate

Using Verilog HDL, a 32-bit ALU with Normal and Re- versible logic gates will be developed. At the conclusion, speed, power, and area (the number of LUTs) parameters of ALUs created using both conventional and reversible logic gates are compared. An ALU with reversible gates—such as Peres, Feynman, and other gates—will be used, which reduces power

consumption and delay and boosts circuit performance.
One XOR, one OR, one NOT, and three AND gates are required for this 3 x 3 reversible gate. Modelsim is used to simulate the design, and Xilinx is used to synthesise it.

V. SIMULATION SYNTHESIS AND POWER RESULTS

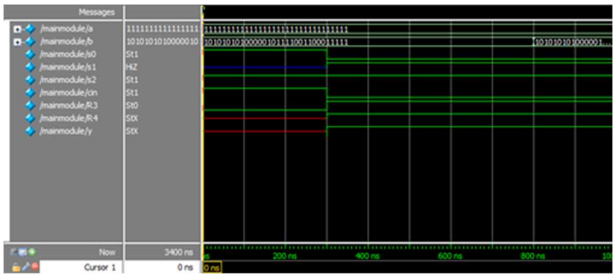


Fig. 8. Simulation of 32-Bit Normal Arithmetic Logic Unit

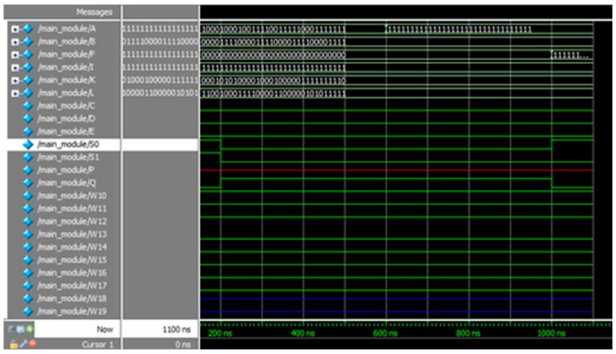


Fig. 9. Simulation of 32-Bit Reversible Arithmetic Logic Unit

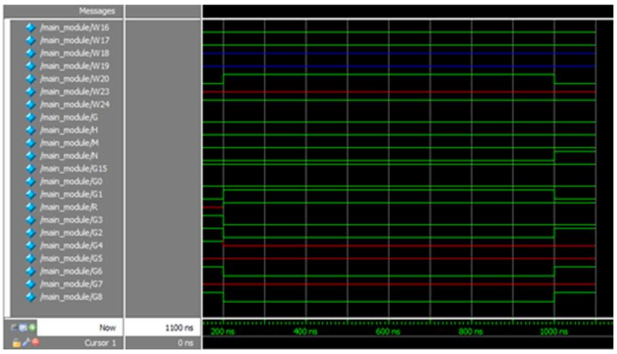


Fig. 10. Simulation of 32-Bit Reversible Arithmetic Logic Unit

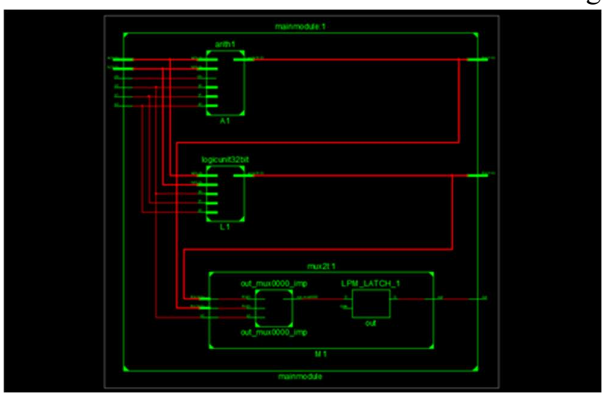


Fig. 11. Synthesis of 32-Bit Normal Arithmetic Logic Unit

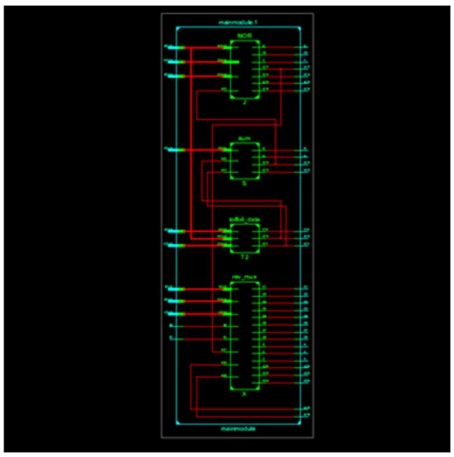


Fig. 12. Synthesis of 32-Bit Reversible Arithmetic Logic Unit

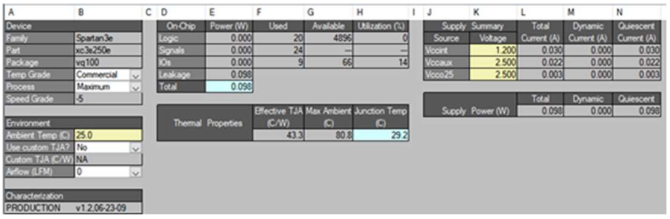


Fig. 13. Power Report of 32-Bit Normal Arithmetic Logic Unit

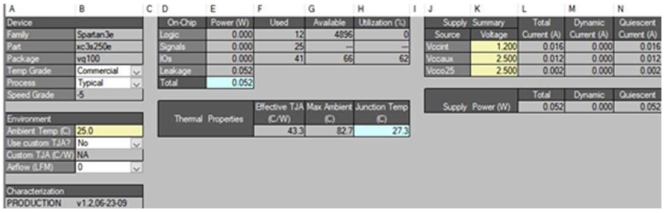


Fig. 14. Power Report 32-Bit Reversible Arithmetic Logic Unit

TABLE I
COMPARATIVE ANALYSIS OF 32-BIT REVERSIBLE ALU IN TERMS OF DELAY, LUT'S AND POWER

S.NO	TYPE OF ALU	DELAY(ns)	LUT'S	POWER(mW)
1	32-Bit Normal ALU	7.162	4	82
2	32-Bit Reversible ALU	6.236	1	52

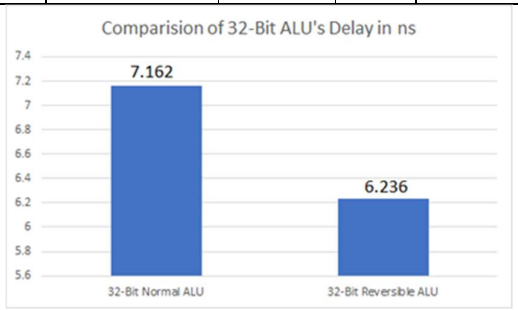


Fig. 15. COMAPARISION OF 32-BIT ALU'S DELAY

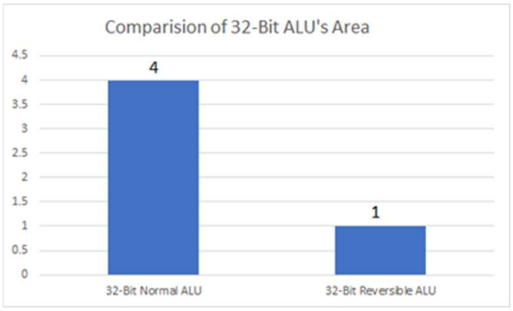


Fig. 16. COMAPARISION OF 32-BIT ALU'S AREA

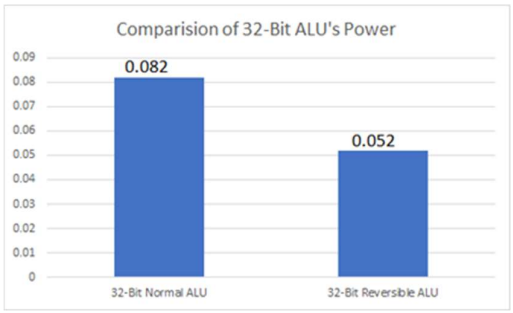


Fig. 17. COMAPARISION OF 32-BIT ALU'S POWER

VI. CONCLUSION

In this research, we used logic gates and reversible logic gates to develop and analyse a variety of ALUs, including 16-bit and 32-bit versions. Reversible gates are utilised in the creation of reversible 16-bit and 32-bit ALUs in place of regular gates. Reversibility reduces power consumption as well as pieces of data are used and lost. Logical reversibility has been the topic of discussion. By employing reversible logic gates, the area, power, and delay of a 32-Bit ALU are all decreased by 25%, 63%, and 87%, respectively. The project's future scope involves using the optimised ALUs.

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