DESIGN AND ANALYSIS OF NOVEL FULL ADDER USING ECRAAL

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Abstract—In VLSI (Very Large Scale Integration) design, adders are digital circuits that perform arithmetic operations, specifically addition, on binary numbers. They are used in many applications, including microprocessors, digital signal processors, and memory systems. An adder is composed of logic gates that take two binary numbers as inputs and produce a binary sum as output. In this paper we have designed and analysed A novel Full Adder circuit by using asychronous adiabatic Logic. ECRAAL means Efficient Charge Recovery Asychronous Adiabatic Logic which combines the ECRL and AAL. ECRAAL is used for implementing Full Adder circuit. The designed ECRAAL Full Adder circuit is compared with the existing ECRL adiabatic Logic in terms of speed, area and power. The Full Adder IS implemented by using TANNER Tools for 250nm Technology. The Novel Full adder has shown improvement in performance. It has decreased 14.71% average power and 50.49% maximum power as compared to ECRL.

Index Terms—Half Adder, Full Adder, Adiabatic Logic, Asy- chronous Adiabatic Logic, ECRL.

I. INTRODUCTION

In VLSI (Very Large Scale Integration) design, adders are digital circuits that perform arithmetic operations, specifically addition, on binary numbers. They are used in many applications, including microprocessors, digital signal processors, and memory systems.

An adder is composed of logic gates that take two binary numbers as inputs and produce a binary sum as output. The simplest adder is a half-adder, which adds two single binary digits, but can only produce a sum of 0 or 1. A full-adder, on the other hand, can add three binary digits (two inputs and a carry from a previous addition) and produce a sum of 0, 1, or 2. However, since binary numbers only use 0 and 1, a full-adder must include additional logic to handle the carry, which is the value carried over from one addition to the next.

There are different types of adders, including ripple-carry adders, carry-lookahead adders, carry-select adders, and carry- skip adders. Each has different characteristics and trade-offs in terms of performance, area, and power consumption. For example, ripple-carry adders are simple and easy to design, but they have a slow propagation delay and require many stages to add large numbers. Carry-lookahead adders, on the other hand, can add large numbers with fewer stages, but they require more complex circuitry and consume more power.

Overall, adders are an essential building block in VLSI design, and their performance and efficiency play a crucial role in the overall performance of digital systems.

II. HALF ADDER

A Half adder is basic adder circuit the adds two input bits and gives sum and carry output bits. The Figure 1 shows Half Adder block diagram. It has A and B inputs and outputs Sum and Carry. The output Sum is one and carry is zero if any one of the input is one and if both inputs are one then the sum is zero and carry is one, if both inputs are zero then sum and carry both are zero. The Table I shows the truth table of Half adder circuit.The Figure 2 shows Half Adder circuit diagram implementation using one xor gate and and gate.

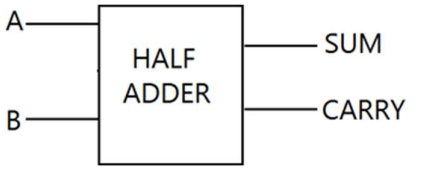


Fig. 1. Half Adder

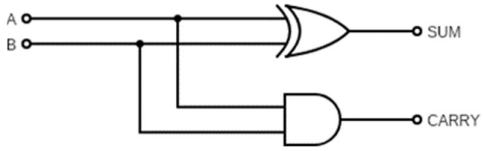


Fig. 2. Half Adder

III. FULL ADDER

Full adder has three inputs and two outputs Sum and Carry. The Figure 3 shows Full Adder block diagram.

TABLE I
HALF ADDER TRUTH TABLE

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The output Sum and Carry is zero when all the inputs are zero, The output Sum is one and Carry is zero when any one of th einput is one,The output Sum is zero and Carry is one when any two inputs is one and The output Sum is zero and Carry is one when all the three inputs are one.

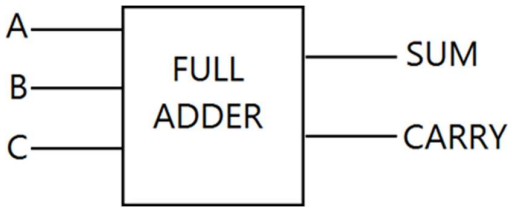


Fig. 3. Full Adder

TABLE II
FULL ADDER TRUTH TABLE

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

IV. ECRL

Efficient Charge Recovery Logic (ECRL) is a technique used in the design of power management circuits for electronic devices. It is used to improve the efficiency of the power management circuitry and to extend the battery life of portable electronic devices.

ECRL works by recovering the charge that is normally lost during the power management process. In a typical power management circuit, when a battery is used to power a device, some of the energy is lost due to the voltage conversion process. ECRL takes advantage of this energy loss by capturing the energy and storing it in a capacitor for later use.

The recovered charge can be used to power the device directly or can be stored in the battery to extend its life. ECRL can also be used to reduce the heat generated by the power management circuitry, which can further improve the efficiency of the device.

ECRL is often used in conjunction with other power management techniques, such as voltage scaling, power gating, and adaptive voltage positioning, to create a highly efficient and effective power management system. The use of ECRL can lead to significant improvements in battery life, which is especially important for portable electronic devices that rely on battery power.

Efficient Charge Recovery Logic (ECRL) offers several advantages in the design of power management circuits for electronic devices:

Improved Efficiency: ECRL recovers the charge that is normally lost during the power management process, which results in improved energy efficiency. This means that less energy is wasted during voltage conversion, and more energy is available to power the device or extend the battery life.

Longer Battery Life: By recovering and storing lost charge, ECRL can extend the life of the

battery. This is particularly important for portable electronic devices, which often have limited battery life.

Reduced Heat Generation: The recovered energy can be used to power the device directly, which reduces the load on the power management circuitry and can lower the heat generated by the circuitry. This can lead to improved reliability and longer device lifespan.

Flexible Design: ECRL can be used in conjunction with other power management techniques, such as voltage scaling and power gating, to create a highly efficient and effective power management system. This allows designers to create customized power management solutions that meet the specific needs of their devices.

Cost-Effective: ECRL is a cost-effective technique for improving the efficiency of power management circuits. Because it is based on capturing and storing energy that is normally lost, it does not require significant additional hardware or components. This makes it an attractive option for device manufacturers looking to improve the energy efficiency of their products.

Overall, the use of ECRL in power management circuits can lead to significant improvements in energy efficiency, device performance, and battery life.

While Efficient Charge Recovery Logic (ECRL) offers several advantages in the design of power management circuits for electronic devices, there are some potential disadvantages to consider:

Complexity: Implementing ECRL can require additional circuitry, which can make the design of power management circuits more complex. This can make it more difficult to design and test the circuits, which can increase development time and costs.

Increased Circuit Size: ECRL requires the use of a capacitor to store the recovered energy. This can increase the size of the power management circuit, which can be a disadvantage for devices where space is limited.

Reduced Voltage Headroom: The use of ECRL can reduce the voltage headroom available in the power management circuit. This can limit the range of voltage levels that can be supported by the circuit, which can be a disadvantage in some applications.

Limited Efficiency Improvement: The benefits of ECRL may be limited in certain scenarios where energy loss during voltage conversion is already minimized. In such cases, the additional complexity of implementing ECRL may not be worth the relatively small efficiency improvement.

Capacitor Leakage: The capacitor used in ECRL may experience leakage over time, which can result in energy loss and reduced efficiency. This can be mitigated through the use of high-quality capacitors, but this can increase the cost of the circuit.

Overall, the advantages of ECRL generally outweigh its potential disadvantages, but the decision to use ECRL should be based on the specific needs and requirements of the device being designed.

A functional N block and two cross-coupled PMOS transistors make up the circuit. Due to the circuit's basic partial adiabatic logic design, it has some restrictions. When the power supply exceeds the transistor threshold value, the two cross-coupled PMOS transistors cease to function, causing non-adiabatic losses. The transistor is turned off and the recovery path is cut off when the supply voltage exceeds the transistor's threshold voltage. As a result, recovery is not complete. The coupling effect, which can cause the two outputs to conflict, is another drawback of ECRL.

The Figure 7 shows Full Adder block diagram using ECRL.

V. ECRAAL

ECRAAL means Efficient Charge Recovery Asychronous Adiabatic Logic which combines the ECRL and AAL. Efficient Charge Recovery Asynchronous Adiabatic Logic (ECRAAL) is a logic design technique that aims to reduce the power consumption of digital circuits by using adiabatic

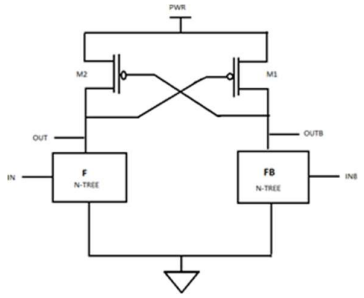


Fig. 4. ECRL

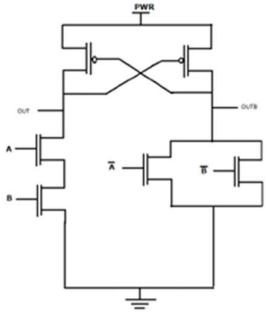


Fig. 5. ECRL NAND GATE

principles. Adiabatic circuits are designed to minimize energy consumption by storing and reusing the energy that is normally lost as heat in traditional circuits.

In ECRAAL, a charge recovery circuit is used to recycle the energy that is dissipated during the switching of the digital circuit. The charge recovery circuit consists of a capacitor and a switch that are used to store and release energy in a controlled manner. During the charging phase of the capacitor, the energy that is normally dissipated as heat is stored in the capacitor.

During the discharging phase of the capacitor, the stored energy is used to power the next stage of the circuit.

Asynchronous design is used in ECRAAL to eliminate the need for a clock signal, which can be a significant source of power consumption in traditional synchronous circuits. In asynchronous design, the different parts of the circuit operate independently of each other, and the timing of the signals is determined by the completion of the previous operation. This eliminates the need for a clock signal, which can result in a significant reduction in power consumption.

ECRAAL is a promising technique for low-power digital circuit design, and has been shown to be effective in reducing power consumption by up to 90% compared to traditional synchronous circuits. However, it is still an area of active research, and further work is needed to optimize its

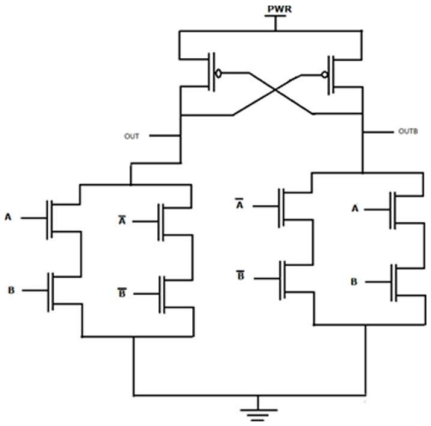


Fig. 6. ECRL EXOR GATE

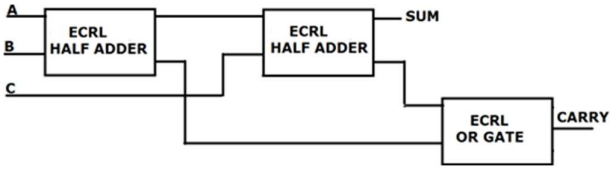


Fig. 7. ECRL FULL AADDER

performance and overcome its limitations.

Efficient Charge Recovery Asynchronous Adiabatic Logic (ECRAAL) has several advantages over traditional synchronous digital circuit design. Some of these advantages include:

Lower power consumption: ECRAAL can significantly reduce power consumption compared to traditional synchronous circuits. By using adiabatic principles to recover and reuse energy that is normally lost as heat, ECRAAL can reduce power consumption by up to 90%.

Higher energy efficiency: ECRAAL can achieve higher energy efficiency than traditional synchronous circuits by recycling energy that would otherwise be wasted as heat.

Asynchronous design: ECRAAL does not rely on a clock signal, which can be a significant source of power consumption in traditional synchronous circuits. Asynchronous design allows different parts of the circuit to operate independently, reducing power consumption and allowing for more flexible and efficient design.

Reduced electromagnetic interference (EMI): ECRAAL can significantly reduce electromagnetic interference (EMI) compared to traditional synchronous circuits. By using asynchronous design and adiabatic principles, ECRAAL can minimize the rapid changes in current and voltage that generate EMI.

Improved reliability: ECRAAL can improve the reliability of digital circuits by reducing the impact of process variations and noise. The adiabatic charge recovery technique used in ECRAAL can compensate for variations in supply voltage and temperature, improving the robustness and reliability of the circuit.

Overall, ECRAAL is a promising technique for low- power digital circuit design, with several advantages over traditional synchronous circuits. However, it is still an area of active research, and further work is needed to optimize its performance and overcome its limitations.

Efficient Charge Recovery Asynchronous Adiabatic Logic (ECRAAL) has some potential disadvantages and limitations that should be considered in digital circuit design. Some of these include:

Complexity: ECRAAL circuits can be more complex than traditional synchronous circuits, especially for large-scale designs. The use of adiabatic principles and asynchronous design can require additional circuitry and design considerations, which can increase the design time and effort.

Limited clock frequency: ECRAAL circuits can have a limited clock frequency compared to traditional synchronous circuits. This is because the adiabatic charge recovery technique used in ECRAAL requires a certain amount of time to charge and discharge the energy storage elements, which can limit the maximum clock frequency of the circuit.

Limited noise immunity: ECRAAL circuits can be more susceptible to noise compared to traditional synchronous circuits. The asynchronous design and charge recovery technique used in ECRAAL can make the circuit more sensitive to noise and other external factors that can affect the timing and operation of the circuit.

Reduced signal speed: ECRAAL circuits can have a slower signal speed compared to traditional synchronous circuits. This is because the asynchronous design used in ECRAAL relies on the completion of the previous operation to determine the timing of the next operation, which can introduce additional delays in the circuit.

Implementation challenges: ECRAAL can be more difficult to implement in practice compared

to traditional synchronous circuits. The additional circuitry and design considerations required for ECRAAL can make it more challenging to design, fabricate, and test the circuit.

Overall, ECRAAL is a promising technique for low- power digital circuit design, but it has some limitations and challenges that must be considered in circuit design. It is important to carefully evaluate the trade-offs between power consumption, performance, and complexity when choosing a circuit design technique for a particular application.

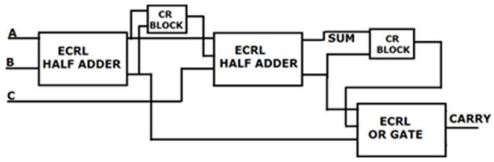


Fig. 8. ECRAAL FULL AADDER

The Figure 7 shows Full Adder block diagram using ECRAAL.

VI. RESULTS

The Figure 9 shows the input and output simulated wave- forms of ECRL Full Adder. The Figure 14 shows the input and output simulated waveforms of ECRAAL Full Adder.

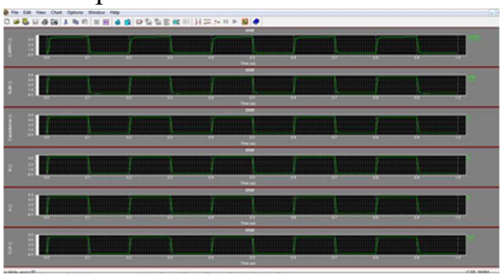


Fig. 9. ECRL FULL ADDER SIMULATED WAVEFORMS

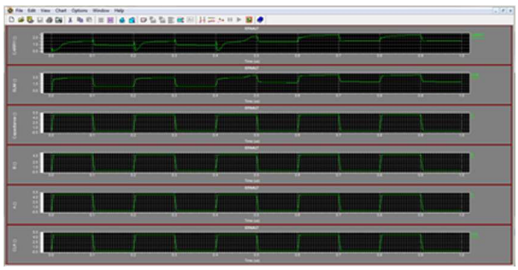


Fig. 10. ECRAAL FULL ADDER SIMULATED WAVEFORMS

VII. CONCLUSION

Thus it can be seen that the praposed ECRAAL Logic has decreaced 14.71 % average power and 50.49 % maximum

TABLE III FULL ADDER

SNO	LOGIC	NO OF TRAN-SIS-TORS	DELAY (pS)	AVERAGE POWER	MAX POWER	MIN POWER
1	ECRL	74	511.97	0.265mW	0.406mW	0.25pW
2	ECRAAL	76	525.73	0.226mW	0.201mW	0.25pW

TABLE IV POWERS DELAY PRODUCT

SNO	LOGIC	DELAY (pS)	POWER(mW)	POWER DELAY PRODUCT (pS * mW)
1	ECRL	511.97	0.265	135.67205
2	ECRAAL	525.73	0.226	118.81498

power as compared to ECRL. The disadvantage is that there is increase of 2.7 % in size of the circuit and 2.68 % increase in delay of ECRAAL as compared to ECRL. But there is 12.42 % decrease of power delay product in ECRAAL as compared to ECRL.Hence we can conclude that ECRAAL is better than ECRL for low power requirements since logic with less power delay product is recommended for low power applications.

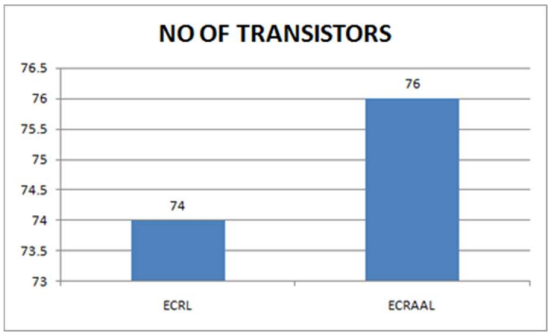
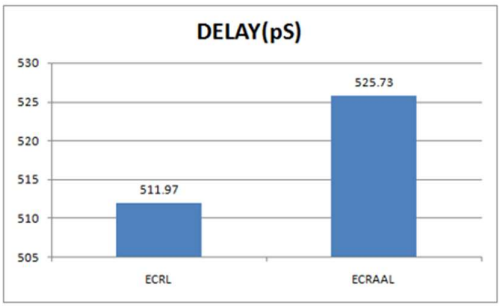


Fig. 11. NO OF TRANSISTORS IN ECRL AND ECRAAL



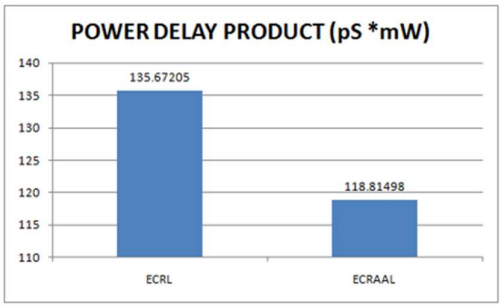


Fig. 12. DELAY IN ECRL AND ECRAAL

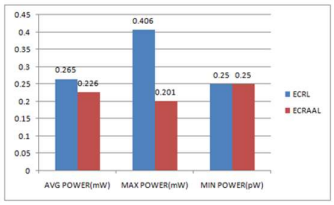


Fig. 13. POWER IN ECRL AND ECRAAL

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