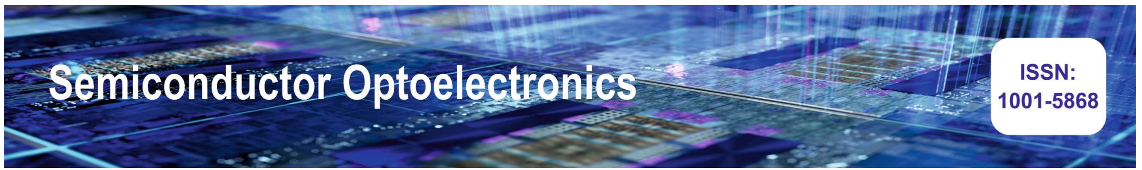

PCBA COMPONENT FAULT IDENTIFICATION THROUGH THE STATISTICAL ANALYSIS OF THE IMAGE.

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Abstract— In modern days, there is a enormous demand for the Printed Circuit Boards with surface mount and through hole components due to its application in various compact and small size consumer electronic gadgets. Hence developing of non-defective Assembled Circuit Board has extended a lot of significance. This research work is primarily concentrating on the recognition of most frequently arising faults in assembled Printed Circuit Boards like missed component, component shifting, upside mount, tombstone and wrong solder joints. In this paper, a process is established for the examination of physical assembled Printed Circuit Boards faults. In this method the position of all components existing in the board is extracted by Fast normalized cross correlation template matching technique. Based on analysis of the Histogram of the extracted components, statistical model is developed to detect the faults. Finally, the position of the identified fault will be marked on the test PCB image so that testing engineer easily observe the position of the defect. The investigation shows that the suggested process effectively accomplishes the recognition and localization of both component and solders joints defects with a minimum detection time of around 321.97msec and also results in 96.25% of accuracy.
Index Terms—Assembled Printed Circuit Board, Surface Mount Component, Through Hole Component, Template Matching, Histogram, Image statistics.

INTRODUCTION

Printed Circuit Board Assembly (PCBA), well-known as PCB assembly, consists of surface mount (SMT) and through components reliant on the need. Through-hole components will be positioned on the PCB using manual techniques by trained technicians. SMT component distribution is divided into three steps. The first of these is screen printing, in which a computer-programmed machine is used and solder paste is applied to the pads on which the product is placed. The next step is to use a computer-aided robot to place the object in a specific location and apply the paste. PCBA is the backbone of every electronics products and is used in many fields such as aerospace, medical and automotive. The performance and durability of all these products depend on the placement of components within the PCB. Therefore, an inspection of PCBA product is an important task in PCB Production. Now in a small business it is very difficult to analyze the site using manual methods. In the industrial sector, inspection of equipment is carried out using expensive optical equipment [1-3]. The aim of this work is to

develop a low-cost analysis system using simple image analysis techniques.

The content of the article is prepared as follows. Section II provides a case study of existing methods for examining PCBA faults that support the development of an efficient process. Section III covers TH and SMT packages and related faults. Section IV shows how to extract the position of all components existing on the circuit board by analyzing the features to detect PCB faults such as missing items, spare parts, flipping chip, tombstones, billboards, improper soldering and marking of fault on the PCB. Then in Part V, the data used and findings of the PCBA inspection are described and the results are analyzed. Lastly, inferences are drawn

LITERATURE SURVEY

EK Teoh et al. Five independent algorithms were developed to detect missing parts, incorrect parts, faulty parts, and faulty connections. PCB competition is important for accuracy[4]. Hong Hailuo et al. A slope plot surface image approximation method for joints is proposed. According to the visual, joints can be divided into two: non-adhesive joints and adhesive joints[5]. A. J. Crispin et al. Methods for finding and identifying more than one object of the same species are being studied using genetic algorithms. It gives the location of the objects found together with its angle of rotation[6]

K Sundaraj presented the process by background subtraction to identify only missed and miss placed capacitor and Integrated circuit. A enormous existence of background pixels will specify fault in the doubted location. This method does not deliver agreeable outcomes if both the component and background of the board are same [7]. Zhou Zeng established a system for getting PCB parts based on spreading of color in focus areas. Trace and recognized the parts by carrying out solder joint and caring coat abstraction. solder joint abstraction contains finding of focus area by specular discovery, identify and eliminate unacceptable focus parts based on color spreading structures. Caring coat abstraction contains grouping of all solder joints of every parts by finding the path of joints of the solder. The method of forming focus pixels by GMM is time overwhelming. Upcoming work might emphasis on refining the efficacy of system [8].

Jiquan Ma et al. recommended a fault recognition technique for PCBA based on apparent reconstruction using a linear mixture of best diffuse and specular reflectance models. From the calculated three joint angles, the solder amount was determined as high, normal or low [9]. N S S Mar et al. classified the joints using individually discrete cosine transform, discrete wavelet transform and Log Gabor filter. Used the mixture of all three methods which is known as classifier fusion for higher recognition rate than the individual methods [10].Csaba Benedek proposed a system to extract, isolate and identify the revelation item of the solder paste. Based on the revelation item, finding short circuit fault in-between the two solder gums by Hierarchical Marked Point Procedure [11]. Feng Xie et al. suggested a technique to identify printed circuit board parts placement faults by genetic programming. It not only identifies the faults but similarly provides wrong positive areas, parts and categories. This technique does not need information of the circuit board design [12]. They auxiliary upgraded the system to identify the faults beneath diverse resolution and illumination disorder [13]. Fupei et al. suggested a technique to identify and categorize solder joint faults using pigment gradients and Boolean instructions. From the structures of the joints, prototypes of solder joint categories

were made to identify missed component and joints faults only [14].
Ganavi et al. suggested three approaches: Subtraction of Background, matching of templates and wavelet transform for faults recognition and categorization in assembled circuit board. These approaches effectively find missed and miss placed parts, no populace, region faults, upside stand, headstone and side projection faults. From the investigation it is apparent that wavelet transform gives the better result. It flops to offer the facts about the category of faults and its locality [15].
Leong Kean Cheong et al. suggested system which uses CNN for finding and locating the circuit board parts faults. Firstly they identify the numerous kinds of parts exist on the circuit board by applying CNN classifier. Secondly they used quicker R-CNN for finding and locating the faults. They also examine that the VGG-16 method offers the good outcome of part identification than InceptionV3 and DenseNet169 methods. They effectively identified 25 dissimilar parts but might identify and locate missed resistor fault only [16]. Mei Zhang et al. proposed a method which uses the deep CNN for one class classifier to detect the fault imageries. They have deep trained CNN model by creating a function based on Euclidean distance. One class of classifiers classifies images as defective or non-defective depending on the radius of the hyper sphere. They conducted an experiment on single electron images only and the results showed that the one-class classifier outperformed the two-class classifier [17]

M.H. Annaby et al. A method has been found to place missed Integrated circuits on circuit boards using the development of similar relationships. They first transform two-dimensional images into one-dimensional vectors, then enhance the one-dimensional vector with spatial domain statistical features to obtain one dimensional feature descriptors, then use DCT to enhance a dimensional vector, and finally use a normalized vector. As a starting point for classifying circuit boards as bad or poor, the dimensionality of the characteristics of the difference between the resulting variables is described [18].
A solo bond joint inspection method was proposed by Nian Cai et. al. and the ViBe algorithm was used to classify solder defects into qualified and non-qualified. Verification time was 903,57ms. The authors further improved their study using the powerful PCA algorithm. They classified solder joints as bad or good without providing details about the nature of the soldering defect: no solder, no solder, added solder, etc. [19-21]. Wenting Dai et al. suggested a profound learning-based algorithm to automatically localize and categorize bond joints of SMT component present on the PCB. This process categorizes the PCB into pass or fail. It fails to detect the many kinds of faults associated with joints of solder like too much solder, too little solder or no solder [22].

CHARACTERISTICS OF ELECTRIC COMPONENTS AND ITS FAULTS

Electrical components are generally classified as inactive components and energetic components. The inactive components include capacitors, resistors, and inductors whereas energetic components include transistors, diodes and Integrated Circuits (IC). Depending on the connection type of the circuit board, components are divided into through-hole and surface mount parts as presented in Figure 1[23]. The through-hole parts can be divided into SIP, DIP and PGA as presented in Figure 2 according to the arrangement of different types of legs such as axial legs, radial legs [23].

Figure 1. Types of electrical component (a) Through-hole (b) SMT

The SMT parts are available in various packages such as Small Outline Integrated Circuit (SOIC), Small Outline Transistor (SOT) , Plastic Leaded Chip Carriers (PLCC), Quad Flat Packs (QFP), Land and Ball Grid Arrays(LGA and BGA) as presented in Figure 3[23]. The SMT component legs may be in the shape of J, L, I, Flat and gull wing. The SOIC and SOT has legs on two sides and are accessible with all kinds of legs shapes. However, PLCC has J shape of legs in four wings and QFP has the Flat shape legs in four wings.

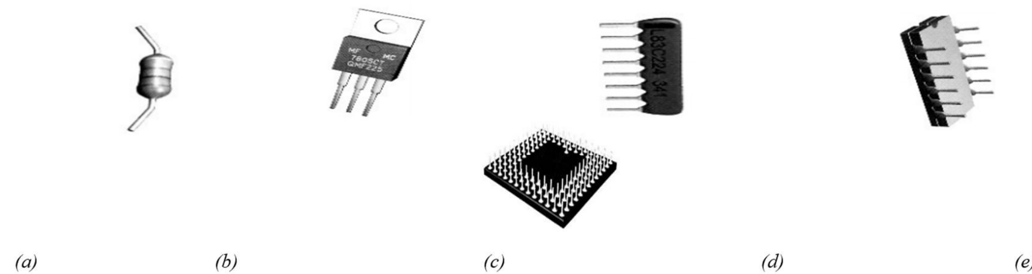


Figure 2. Types of Thruogh-hole parts (a) Axial legs (b) Radial legs (c)SIP (d) DIP (e) PGA

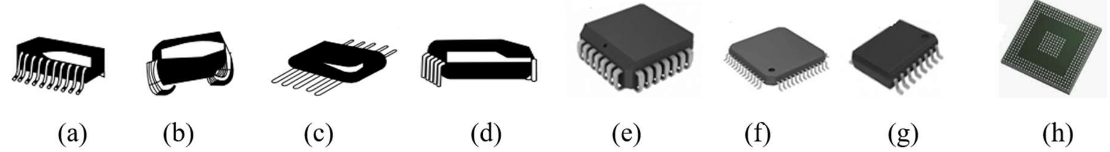
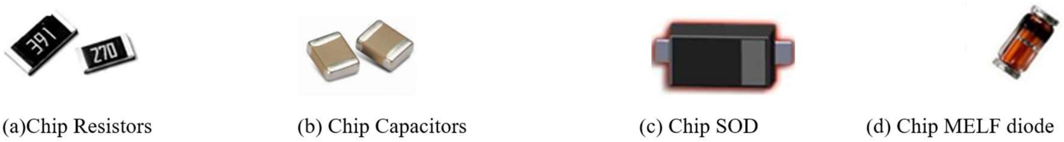


Figure 3. Types of legs and Packages for SMT component (a) Gull wing (b) J leg (c) Flat leg (d) I leg (e) PLCC (f) QFP (g) SOIC (g) BGA

The SMT inactive parts such as resistors, capacitors and semiconductor diodes not contain any legs. Instead they contain metalized end as presented in Figure 4 and are called as chip components. Among the SMT components available in the market 80% of the components belong to the type of chip components. The diodes are accessible in two kinds of packages. They are Small Outline Diode (SOD) which is commonly used to control low power intemperance and Metal Electrode Face Bonded (MELF) which is normally used to control high power necessity. All the components or packages deliberated in this segment are accessible in different sizes.

The faults arising throughout the manufacturing of bare circuit board are connected to the land outline of the component and the electric wiring construction among the components via the copper trace. But the faults arising in the PCBA are fully connected to the components as showed in Table I. These faults are classified as solder defects such as less solder(LS), no solder(NS) and excess solder(ES) and component defects such as component missed(CM), component shifting(CS), upside mount(UM), tombstone(TS) etc.



(a)Chip Resistors (b) Chip Capacitors (c) Chip SOD (d) Chip MELF diode

Figure 4. Types of surface mount chip components

All types of faults excluding component shifting, upside mount and tombstone are relevant for both SMT and TH components. If the component is attached upright at one end and detached at the other end then it signifies the tombstone fault. In Table I 'A' and 'NA' signifies whether the respective fault is "applicable" or "not applicable" for the specific component in that order. This Table comprises the list of frequently arising faults during the manufacturing of PCBA. This investigation address all the faults indicated in the Table I for the chip components and only missed component and component shifting faults for the remaining components.

TABLE I. FREQUENTLY ARISING FAULT IN PCBA

Sl. No.	Image of the Component	Type of Package	Soldering Faults			Components Faults				
			LS	NS	ES	CM	CS	UM	BB	TS
1		Capacitor chip	A	A	A	A	A	A	A	A
2		Resistor chip	A	A	A	A	A	A	A	A
3		MELF Diode	A	A	A	A	A	NA	NA	A
4		SOD	A	A	A	A	A	A	A	A
5		SOT,SOIC, QFP	A	A	A	A	A	A	NA	NA

PROPOSED MODEL

Many researchers proposed the method for identifying either component defects or solder joint defects. The identification and localization of both solder joint and component placement defects for all the existing component in the whole assembled PCB is a challenging task.
The suggested system will recognize and localize both solder joint and component placement defects. In the suggested system there are two parts. The first one is feature extraction and the second one is fault identification. In the first part the region of each the components existing in the non-defective sample board is extracted using template matching. The Table II shows the position of the extracted components existing in the non-defective sample board presented in Figure 5.

TABLE II.REGION OF THE EXTRACTED COMPONENT FOR THE SAMPLE PCBA IMAGE

Sl. No.	Extracted Component	Height of the component	Width of the component	Position of the component			
				Corner1 coordinates(x1,y1)		Corner2 coordinates(x2,y2)	
1		36	88	102	156	190	192
2		66	32	482	102	514	168
3		66	32	564	12	596	78
4		88	36	144	40	184	128
		36	88	404	26	492	62
		36	88	220	156	308	192
5		72	58	218	34	276	106
		72	58	318	40	376	112
		72	58	550	120	608	192

6		36	88	364	148	452	184

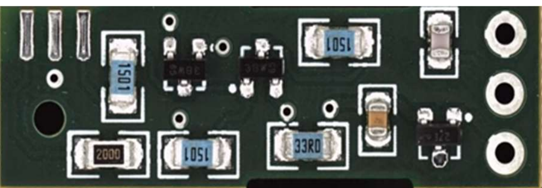


Figure 5. Non-defective sample PCBA

As soon as the position of the components extracted, position of the solder joints for the chip components presented in Table III will be extracted using width, height and two diagonal corner points((x1,y1) and (x2,y2)) of the components. If height of the component greater than the width of the component then equation 1 and 2 else equation 3 and 4 will be used to extract the solder joints of the component. In general the chip component includes two solder joints. Here solder joint1 and joint 2 is indicated by ((j1_x1, j1_y1) and (j1_x2, j1_y2)) and ((j2_x1, j2_y1) and (j2_x2, j2_y2)) respectively.

$$\left.\begin{array}{l} j1_x1 = x1 \\ j1_y1 = y1 \\ j1_x2 = x2 \\ j1_y2 = y2 + \frac{height}{4} \end{array}\right\} \quad (1)$$

$$\left.\begin{array}{l} j2_x1 = x1 \\ j2_y1 = y2 - \frac{heigh}{4} \\ j2_x2 = x2 \\ j2_y2 = y2 \end{array}\right\} \quad (2)$$

$$\left.\begin{array}{l} j1_x1 = x1 \\ j1_x1 = y1 \\ j1_x1 = x1 + \frac{width}{4} \\ j1_x1 = y2 \end{array}\right\} \quad (3)$$

$$\left.\begin{array}{l} j2_x1 = x2 - \frac{width}{4} \\ j2_x1 = y1 \\ j2_x1 = x2 \\ j2_x1 = y2 \end{array}\right\} \quad (4)$$

The histogram of every component existing in the non-defective board and defective board under test will be obtained. The statistical model developed through the study of histogram of

components existing in the non-defective sample board and defective board under test for finding the faults.

The image statistics S1 and S2 can be found for all components existing in non-defective circuit board by histogram of the component using equation 5 and 6 respectively. The S3 can be found for the solder joints of all components by the histogram of the solder joints using equation 7. The value of S1, S2 and S3 should be calculated for non-defective components which are indicated by S1ND, S2ND and S3ND respectively. Similarly the value of S1, S2 and S3 should also be calculated for components under test which are indicated by S1TestC, S2 TestC and S3 TestC respectively.

$$S1 = \sum_{i=250}^{255} i * ki \qquad (5)$$

$$S2 = \sum_{i=50}^{140} i * ki \qquad (6)$$

$$S3 = \sum_{i=240}^{255} i * ki \qquad (7)$$

TABLE III. REGION OF SOLDER JOINTS OF CHIP COMPONENT

Sl. No.	Chip Components with two solder joints	Region of Solder Joint1		Region of Solder Joint2	
		Corner 1 (j1_x1,j1_y1)	Corner 2 (j1_x2,j1_y2)	Corner 1 (j2_x1,j2_y1)	Corner 2 (j2_x2,j2_y2)
1		(102,156)	(124,192)	(168,156)	(190,192)
2		(482,102)	(514,118)	(482,152)	(514,168)
3		(564,12)	(596,28)	(564,62)	(596,78)
4		(144,40)	(180,62)	(144,106)	(180,128)
		(404,26)	(426,62)	(470,26)	(492,62)
		(222,156)	(244,192)	(288,156)	(310,192)

5	33R0	(364,148)	(386,184)	(430,148)	(452,184)

The range of i is decided based on the comparison of histogram curve of non-defective and faulty component. The comparison of histogram curve of non-defective component with that of different faulty components specifies that the amount of the pixels whose intensity value ranging from 250 to 255 for upside mount and bill board fault component is very huge compared to that of non-defective component as presented in Figures 6 and 7. Hence S1 is used for finding the upside-mount and bill-board fault.

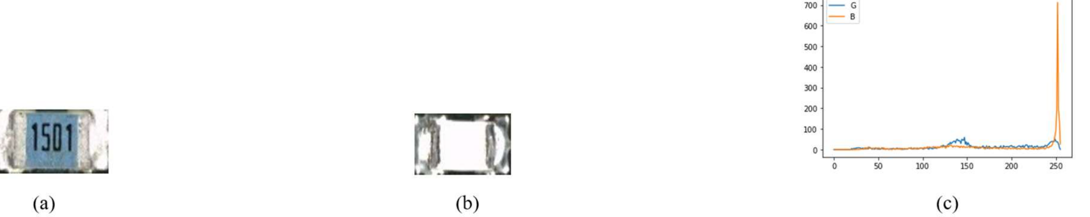


Figure 6. Histogram comparison for non-defective component with upside mount defect component(a) Non-defective component (b) upside mount component (c) comparison of grey level intensity of (a) & (b)

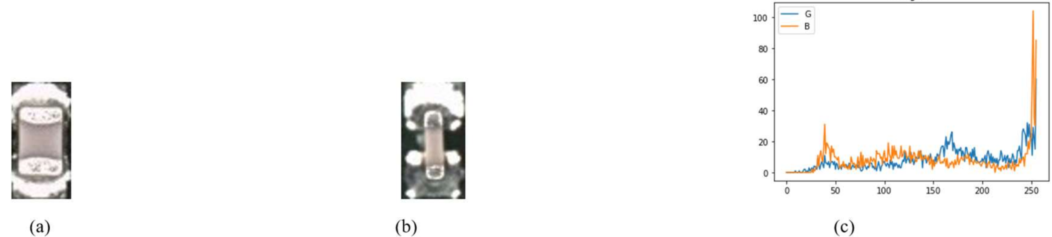


Figure 7. Histogram comparison for non-defective component with Bill Board defect component (a) Non-defective component (b) Bill Board component (c) comparison of grey level intensity of (a) & (b)

After fixing each component on the circuit board by applying the solder paste at particular location, the circuit boards are treated inside the reflow machine under high temperature. During this process, the horizontally fixed chip components may change the direction to upright and it is deliberated as tomb stoning fault. The non-defective component, tomb stoning component and their histogram are presented in Figure 8. The histogram specifies that the Tomb stoned component has more quantity of pixels whose value ranges from 50 to 140 (Black shade pixels) compared to that of the non-defective component. Hence S2 is used for the finding the tomb stone fault. Similarly S3 is used for ruling the solder joint faults.

Figure 8. Histogram comparison for non-defective component with Tomb stoning defect component (a) Non-defective component (b) Tomb stoning component (c) comparison of grey level intensity of (a) & (b)

The Second part of the suggested method is finding and locating of the faults. The value of UM_BBC got using equation 8 can be used to find the upside mounts and Bill Board faults UM_BBF based on the conditions given in equation 9. The value ranging from -0.5 to 0.5 indicates No Fault(NF), between -3 to -0.5 specifies Bill Board fault(BBF), less than -3 specifies Upside mount component fault (UMF). Also the values of all the statistical parameters for non-defective component are fewer matched to that of upside mount component and bill board component as presented in Table IV and V.

$$UM_BB_C = \frac{S1_{NDC} - S1_{TestC}}{S1_{NDC}} \quad (8)$$

$$UM_BB_F = \begin{cases} \text{UMF} & \text{UD}_{\text{BB}_\text{C}} < -3 \\ \text{BBF} & -3 \leq \text{UD}_{\text{BB}_\text{C}} < -0.5 \\ \text{NF} & \text{UD}_{\text{BB}_\text{C}} \geq -0.5 \end{cases} \quad (9)$$

The Tomb stoning fault can be recognized using the equation 10 .The value of 〖TS〗_C less than -1 indicates the Tombstone defect as displayed in Table VI. The value of SJC got using equation (11) can be used to find and classify the various solder joint fault indicated by SJF as extra solder(ES), less solder(LS), no solder(NS) and good solder(GS) based on condition presented in equation (12).

$$TS_C = \frac{S2_{NDC} - S2_{TestC}}{S2_{NDC}} \quad (10)$$

$$SJ_C = \frac{S3_{ND} - S3_{TestC}}{S3_{ND}} \quad (11)$$

$$SJ_F = \begin{cases} ES & SJc < -0.2 \\ GS & -0.2 \leq SJ_C \leq 0.2 \\ LS & 0.2 < SJ_C < 0.8 \\ NS & SJ_C \geq 0.8 \end{cases} \quad (12)$$

TABLE IV. COMPARISON OF GOOD COMPONENT WITH UPSIDE MOUNT COMPONENT BASED ON PIXEL INTENSITY AND ITS SUM

Pixel intensity (i)	Pixel count (ki)					
	Reference PCB good component	Test PCB upside mount component				
		1	2	3	4	5
250	33	70	84	71	83	86
251	38	104	121	156	108	92
252	29	488	438	506	241	238
253	46	188	225	204	145	130

254	11	104	122	106	115	110
255	1	14	18	12	17	22
$S1 = \sum_{i=250}^{255} i * ki$	39783	244130	254250	266014	178820	171008
$UM_BB_C = \frac{S1_{NDC} - S1_{TestC}}{S1_{NDC}}$		**-5.1365**	**-5.3909**	**-5.6866**	**-3.4948**	**-3.2985**

TABLE V. COMPARISON OF GOOD COMPONENT WITH BILL BOARD COMPONENT BASED ON PIXEL INTENSITY AND ITS SUM

Pixel intensity	**Pixel count (ki)**					
	Reference PCB good component	**Test PCB bill board component**				
		1	2	3	4	5
250	33	40	42	45	37	41
251	38	39	58	48	68	52
252	29	60	55	64	104	82
253	46	62	93	67	73	64
254	11	80	88	98	78	91
255	1	17	24	17	25	21
$S1 = \sum_{i=250}^{255} i * ki$	39783	75250	90919	85604	97182	75575
$UM_BB_C = \frac{S1_{NDC} - S1_{TestC}}{S1_{NDC}}$		**-0.8915**	**-1.2853**	**-1.1517**	**-1.1442**	**-0.8996**

TABLE VI. COMPARISON OF GOOD COMPONENT TOMB STONE COMPONENT BASED ON PIXEL INTENSITY AND ITS SUM

Component		$S2 = \sum_{i=50}^{140} i * ki$	$TS_C = \frac{S2_{NDC} - S2_{TestC}}{S2_{NDC}}$
Non-defective board Component (S_{NDC})		49675	
Test PCB Tomb Stone component (S_{TestC})	1	111257	-1.23
	2	101975	-1.05
	3	106267	-1.139

	4	105105	-1.115
	5	107812	-1.17

Next component missing and shifting defect can be identified by pattern or template matching technique. The data base which is created for the reference board contains position and count of every component present in that board. The fast normalized cross correlation based template matching technique is applied for the non-defective board and the board under test to find the position and count of every component present in both the boards. Then compare the position and count of every component of non-defective board with that of test board to identify the component missing and shifting. If both position and count of the components matches, then there is no component missing and shifting. If count of the particular component matches and position of the component present in the test board not matches with that of non-defective board, then there is component shifting. Next, if count of the component does not matched, then it represents the missing component defect.

EXPERIMENTATION AND RESULTS

Testing of the proposed method to integrate PCB analysis was performed on PC system using Windows8, 64-bit operating system, 6 GB installed memory and Intel core i5 4200U CPU @2.30 GHZ processor. The software used for the application is Python. The camera used to capture the PCB image in the experiment is NIKON D810 with a resolution of 36.0 MP (7360x4912), a full-screen CMOS sensor size of 35.90 mm(h)x24mm(v). To carry out the experimentation defective and non-defective PCBAs are collected from one of the PCBA industry located in Mysore. The experimentation is conducted on 150 boards. Among 150 boards 30 boards contains only Through hole components, 100 boards contains only SMT components and remaining 20 boards contains both Through hole and SMT components. Five different assembled PCBs shown in Figure 9 are used for the experimentation and the details of these boards are depicted in Table VII and VIII. The Table VII represents the number of components presents in every sample boards. Whereas, the Table VIII represents the number and types of defects present in the sample boards.

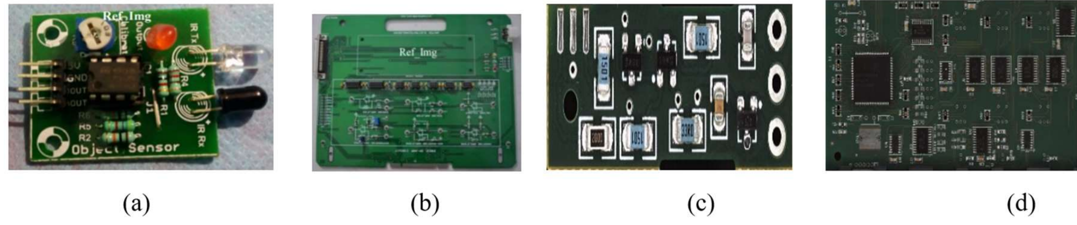


Figure 9. Assembled PCB Samples-(a)Sample1 PCB with only TH components , (b) Sample 2 PCB with only TH components, (c) Sample3 PCB with only SMT components, (d)Sample5 PCB with only SMT components

The presence of component defects such as component missing, component shifting, upside mount, bill board, tomb stoning are identified using model 1 shown in Figure 10. The presence of solder joint defects such as extra, less, No and good solder joints are identified using model 2 shown in Figure 11.

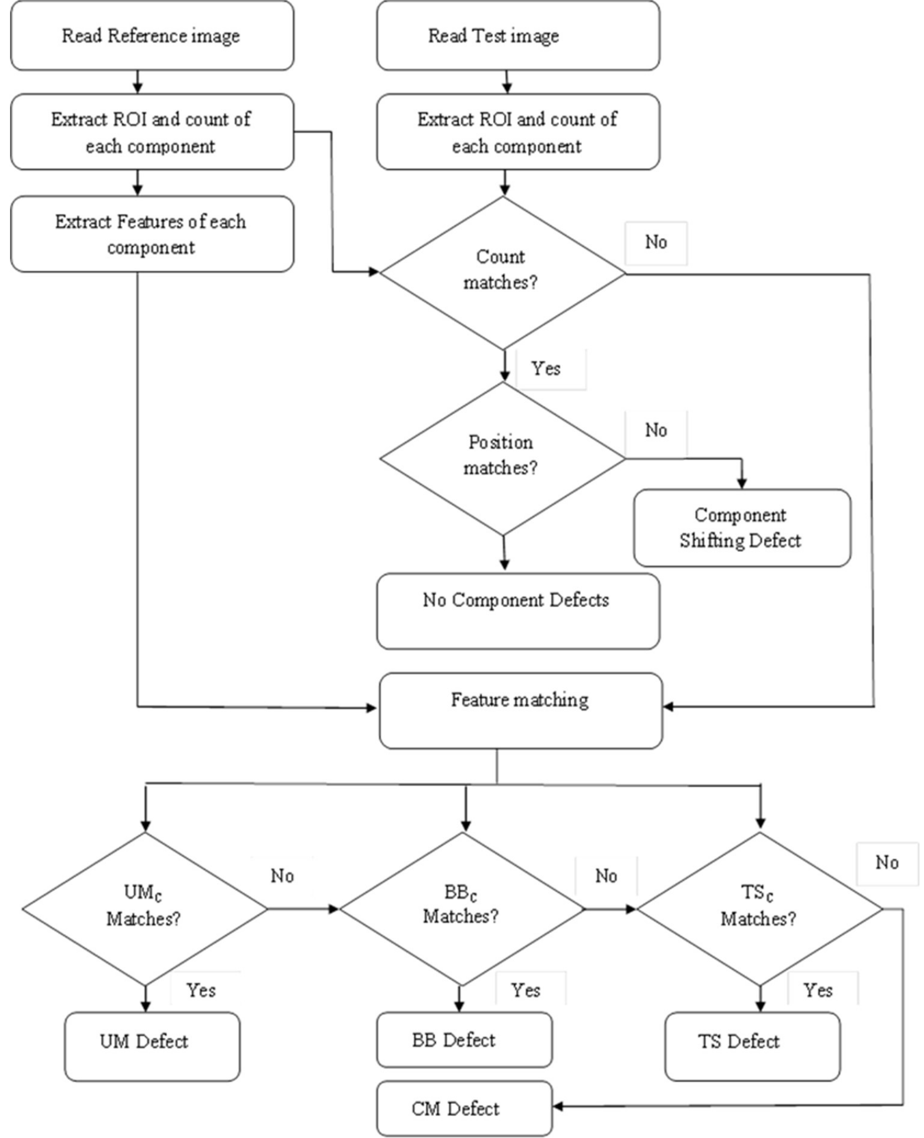


Figure 10. Flow of Component defect detection model

TABLE VII. DETAILS OF TYPE AND NUMBER OF COMPONENT IN ASSEMBLED PCB DATA SET

Dataset	Number of boards	Size of the boards	Number of Components			
			TH	SMT		Total
				Chip Components	SOIC Components	
Sample 1	20	60mmx50mm	14	0	0	14
Sample 2	10	30mmx30mm	8	0	0	8
Sample 3	80	90mmx30mm	0	8	2	10
Sample 4	20	60mmx50mm	0	11	29	40
Total	**130**		**22**	**19**	**31**	**72**

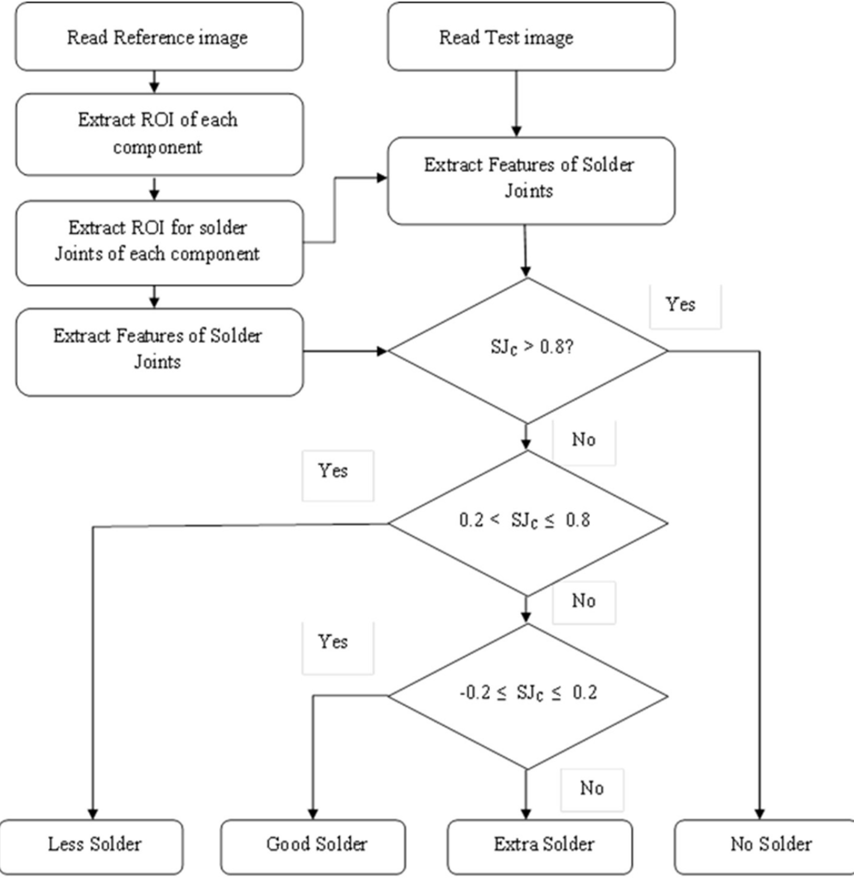


Figure 11. Model for identification of Solder Joint defects

TABLE VIII. DETAILS OF TYPE AND NUMBER OF COMPONENT AND SOLDER JOINT DEFECTS PRESENT IN ASSEMBLED PCB DATA SET

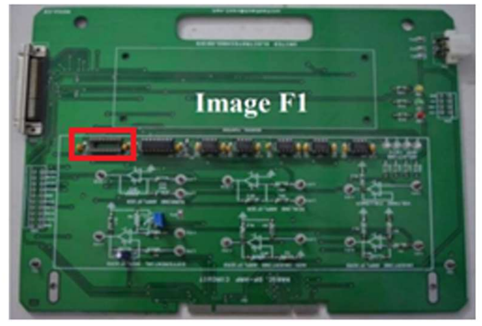
Defect Name	Number of defective boards				Total
	Sample 1	Sample 2	Sample 3	Sample 4	
Component Missing	4	4	0	12	20
Component Shifting	0	0	5	5	10
Upside Mount	0	0	8	0	8
Bill Board	0	0	8	0	8
Tombstone	0	0	8	0	8
Less Solder	0	0	10	0	10
No Solder	0	0	10	0	10
Extra Solder	0	0	6	0	6
Total	**4**	**4**	**55**	**17**	**80**

The Graphical user interface (GUI) for testing the assembled PCB is as shown in Figure 12.

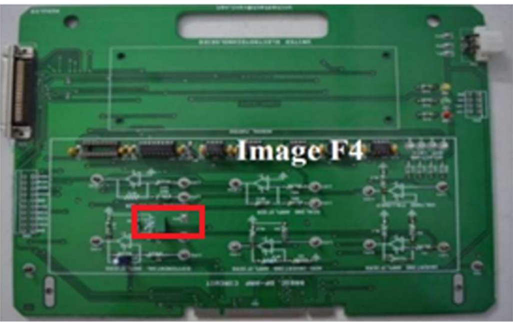
The result window consists of four parts. The first part contains the list of components along with count present in the reference board. The second part contains details of component under test and it includes template of the component, name of the component and count of that component. The third part is provided for displaying the test PCB. The last part is the table which contains component name and its count for the test PCBs. If both the counts and position of all the components are equal to the expected counts and positions, then there is no component related defect. If only the count of the component matches but mismatch in the position of the component, then it indicates the component shifting defect. The mismatch in the count of the component results in only component missing defect for assembled PCBs which contains only through hole component. Whereas the count mismatch results in various other defects such as upside mount, bill board, tomb stoning or component missing defects for the assembled PCBs which contain SMT components.

It is also very important to identify whether the solder joints of the SMT chip component are good or defective in addition to identification of whether the component is good or defective. Figure 13 shows the missing component inspection output for the assembled PCB which contains only TH components and Figure 14 and 15 shows the component and solder joint inspection output for the assembled PCB which contains only SMT components respectively.

Figure 12. Automated PCB inspection result window

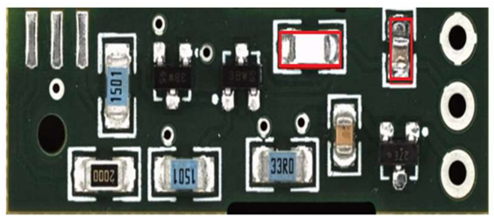


(a) Missing IC

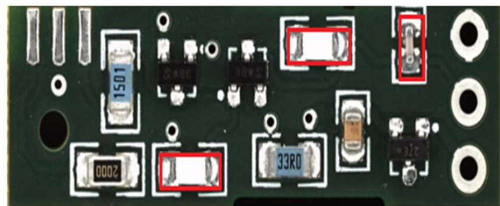


(b) Missing jumper

Figure 13. Missing component inspection output for Through Hole PCBA

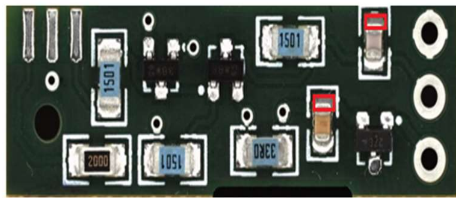


(a)Upside mount and tomb stoning component defect

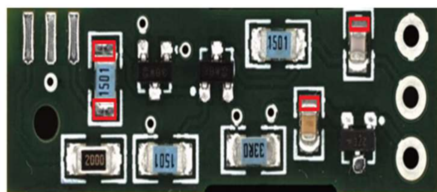


(b) Upside mount and bill board component defect

Figure 14. Component and solder joint defects localization in defective SMT assembled PCBs



(a)No solder – solder joint defect



b)No solder and less Solder – solder joint defect

Figure 15. Component and solder joint defects localization in defective SMT assembled PCBs

The performance analysis of the proposed method is done based on the type of the defects presents (numerical count of the defects) in the board and time taken (speed of detection) for the detection and localization of the defects (defects coordinate position). Cost of the system with respect to the AOI machine is also presented. The time taken for the individual process of the suggested method for the inspection of PCBA is depicted in Table IX. The accuracy of the examination of defects is represented in Table X.

TABLE IX. TIME TAKEN FOR DISTINCT STEPS OF THE PROPOSED METHOD

Sl. No.	Steps	Time in msec.
1	Non-defective board Image read & preprocessing (one time procedure)	0.501
2	Extract the region of the each component and its solder joints in Non-defective board (one time Process)	318.00
3	Extract features of the each component and its solder joints in the Non-defective board (one time Process)	3.002

4	Testing board Image read & preprocessing	0.501
5	Extract the region of the each components present in the board under testing.	317.49
6	Extract features of the each component and its solder joints in the board under testing.	3.002
7	Component associated defect detection	0.480
8	Solder joint associated defect detection	0.501
Total time required for the defect identification including onetime process		**643.477**
Total time required for the defect identification excluding onetime process		**321.974**

TABLE X. INSPECTION ACCURACY OF THE PROPOSED METHOD

Name of the Defect	Total Number of defects	Number of defects identified	Accuracy of defect detection in %
Component missing	20	20	100
Component shifting	10	10	100
Upside mount	8	8	100
Bill board	8	8	100
Tombstone	8	8	100
Less solder	10	9	90
No solder	10	10	100
Extra solder	6	4	66
Total	**80**	**77**	**96.25**

The author also compared the proposed method with the various types of AOI machines presently used in the PCB assembly industries to inspect the assembled PCBs and it is depicted in Table XI.

TABLE XI. PERFORMANCE COMPARISON OF THE PROPOSED METHOD WITH VARIOUS TYPES OF AOI MACHINES USED IN THE INDUSTRIES

Type of the AOI machines/ Proposed method	Approximate Cost	Time taken to inspect the board	Defects identified by the machine/ proposed method	Accuracy in %
Semi-Automatic Optical Inspection (Offline machine)	35 lakh	20- 30 sec	Only Component defects of Chip components and ICs	80%
Fully Automatic Optical Inspection (Online machine)	1.2crores	20- 30 sec	Only Component defects of Chip components and ICs	80%
Automatic X-ray Inspection (AXI)	3.74crores	60 sec	Both component and solder joint defect for all chip components and ICs expect hidden joints of BGA component	95%

Proposed method	2 Lakh	0.322 sec	Both component and solder joint defect for all chip components and only missing and misaligned defects for ICs	96.25%

The semi and fully automatic machines inspect only the component related defects such as wrong part, orientation, on-device marking, bill board, upside down, missing component, component shifting and tomb stoning. The AXI machine inspects all component defects along with all solder joint defects for all components except BGA component. The proposed method also inspects all component related defects except wrong part and orientation and all solder joint defects for all chip components such as resistor, capacitor and semiconductor diodes which covers the 80% of the available components. The accuracy of the proposed method is better compared to existing machines and also the cost and time taken for the proposed method is very less compared to the existing machine.

The Table XII gives a comparison of the proposed method with other existing approaches which based on the complexity of the input board and inspection time. Nian Cai used robust principal component Analysis to inspect the single solder joint image and accurately classified the solder joints into defective or non-defective. But this method takes more time for the inspection [20]. Wenting Dai used deep learning concept YOLO to trace the small solder in assembled PCB images, SVM and K means clustering to classify the solder joints into qualified or defective. The time taken for the inspection of solder joint was 240msec. But the tracing of small objects such as solder joints using YOLO concept resultsin less accuracy [22]. Xie Hongwei used AdaBoost and decision tree concept to inspect the single chip component 0402. Based on the prior knowledge the solder joint was divided into 12 sub regions and features of every sub regions were extracted and evaluated using improved AdaBoost to classify the solder joint into defective and no defective. Finally defective solder joints were categorized as missing, shift, tomb stone, less solder, and pseudo joints using decision tree. This method resulted in 97% of accuracy and has taken 8.6msec for the inspection of single solder joint image. It is difficult to adopt this method for the inspection of the real assembled PCBs which contains more number of chip components of various sizes because dividing of every small chip component present in the board into 12 sub regions and extraction of features from those 12 sub regions will become more complex[28]

TABLE XII. PERFORMANCE COMPARISONS OF THE PROPOSED METHOD VS OTHER METHODS

Sl. No.	Methods	Defects Addressed	Name of the Defect	Printed Circuit Board Image and size	Inspection Time in terms of msec.
1	Robust Principal Component Analysis	Only Solder joint	Classifies the solder joint as either defective solder or Non defective solder	3mmx1mm	2900.0
2	YOLO+SVM+K mean Clustering				340.0
3	ViBe Algorithm				903.57
4	Improved AdaBoost and Decision Tree		missing, shift, tomb stone, less solder, and pseudo joints	3mmx1mm	8.6
5	Background Subtraction	Only Component defect	Upside mount, missing component, misaligned component	24mmx18mm	1620
6	Template Matching				6455
7	Wavelet Transform+ Image Subtraction				1107
8	Proposed System	Both component and solder joint defect	Upside mount, bill board, tomb stoning, missing component, Component Shifting, less solder, no solder, extra solder	90mmx30mm	321.97

Ganavi performed template matching, wavelet transform and background subtraction based direct image comparison of reference PCB and Test PCB to identify only the presence of component related defects such as upside mount, missing component and misaligned component. The time taken for the inspection was very high and also it fails to provide the information about the type of defects and its location [15]. In the proposed method fast normalized cross correlation based template matching and Statistical parameters are used to identify both component and solder joint defects with a minimum inspection time of around 321.97msec. It is experimented on the assembled PCBs which contains only through hole components, only SMT components and both TH and SMT components. Our method identifies more number of the defects commonly occurring in the assembled PCB with a minimum time compared to all other previous method. Hence it can be used for the final stage inspection of board in the assembled PCB manufacturing industries.

VI. CONCLUSION

This research work focuses on the identification of both component and solders joint defects in PCBA. The key notion of the recommended method is to extract the region of each component and its structures to discover the component associated faults such as missing component, shifted component, upside mount, tomb stone and bill board component. Also

extract region of the solder joints of each SMT component and its structures to detect the faults associated to solder joints such as no, less and too high solder. Our model will pinpoint most of the PCBA fault and also delivers the facts about type and position of the fault. The cost of method proposed is very less compared to existing method. The proposed method gives better performance with inspection time of 0.321 sec. In future the researches can focus on the inspection of PCBA for small outline integrated chip component faults.

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