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LOW PROPAGATION DELAY MEMRISTOR LOGIC GATES

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Abstract

The memristor is nevertheless a pretty unknown circuit, performing arithmetic operations. Previously, in almost all the currently working circuits, especially in digital circuits, implementing signal processing applications, basic logical operations such as NAND and NOR are performed on values which are represented by voltages and currents. The drawback in this method is it occupies more space, more time and more power. However, this paper discusses a simple element known as memristor that perform logical operations such as NAND, NOR gates and DFF which occupies less space, less time and less power. Therefore, it is understood that by using the memristor, logical operations in digital circuit is done faster and also saves power because the memristor is non volatile element.

It requires-------less space than conventional based FFs,it is ------ faster than Conventional based FFs, and also it uses ----- less power than conventional based FFs.

It is used widely in electronic Industries.

Keywords: Memristor, Transient Delay, Low Power, Space

INTRODUCTION

For nearly fifty years, enclosed digital circuits designed with semiconductor devices have widespread. This growth has increased orders of significance upgrades in rate, electricity intake, and dependability. These trends are direct consequences of frequent shrinking of tool dimensions inside the semiconductor fabrication system, as at the beginning delineate mistreatment by Gordon Moore in 1965, predicting the rise and proliferation of digital computing and its programs, but, can't be sustained indefinitely. There's broad agreement that nanoscale CMOS semiconductor sizes can reach basic physical limits within the subsequent decade [1]. Each different downside is that the energy disaster related to strength dissipation in pc systems [3], these arduous problems are presently perceived as major disruptions at the organic process direction of computing, occupation for huge investments in analysis to broaden new systems for resultant technology computing systems. The new technologies that will

extend the talents of CMOS are Memristive gadgets. This focuses on Memristive technologies and their impact on computers, an enormous success within the realm of semiconductor gadgets became settled in twentieth century with the creation of transistors. Shrinking of CMOS gadgets into nanoscale regime has led to the usage of multi core architectures in central processor to extend the performance. Memristor is one such tool, it will keep statistics and might conjointly transfer between exclusive states. It is a 2 terminal device, totally different features. There are varieties of future methods in latest technology that finds memristive programs. Memristor reveals applications in fields like analog circuits, neuromorphic systems and logic circuits. Memristors basic belongings is data garage. i.e. it is a memory detail.

The records are kept within the form of resistance specifically the condenser (first accomplished in 1745), the electrical device (1828) and also the coil (1831). While Maxwell declared his illustrious and intensely powerful equations. A few years later, it became clear those three components are direct consequences of this concept that unifies strength and magnetism. However, in 1971 a younger circuit intellect, Leon Chua argued from theoretical grounds that there should be in addition a fourth circuit part that became equally essential because of the opposite 3 [1]. He gave this detail the name Memristor since it, below positive things, acts as a electrical device with memory, i.e. the resistance is looking on the physical history. Within the years following Chua's work. The Memristor plan was left pretty alone till the delivery of technology some years within the past whereas a collection at the Hewlett-Packard (HP) research laboratory managed to assemble a bodily part showing as a Memristor[2,3].

To provide the overall perspectives of numerous applications of Memristor into Discrete devices and Array devices applications. The discrete device applications use memristors in a manner that takes advantage of their nonlinear characteristics and their controllable resistance changes to enhance the performance of the desired applications. Array device applications on the other hand not only depend on memristor properties but are also coupled with the ongoing trend to increase the device density by reduce the width of the wires in nano crossbar structure and also used in nonvolatile memory, neuromorphic circuits, reconfigurable logic ,chaos circuits and Logical gates.

Over the past twenty five years, flash reminiscence primarily based completely on rate stable gear in MOS transistors has been scaled sharply, even surpassing Moore's regulation. Scaling below twenty nm entails daring challenges, these contests become inexcusable, while flash technique technology scales beneath fifteen nm. In recent years, different technologies have been explored to seek out a alternative for flash. The stored data is painted as a resistance and also the garage tool is fancied at intervals the metal layers. those technologies proportion similar homes – nonvolatility, relatively high write patience, excessive density, glorious measurability beneath ten nm, and quick scan and write. Memristors may switch resistance states at a lower voltage levels than the signal voltage levels used in Transistors based in Complementary Metal Oxide Semiconductor (CMOS) technology

Memristor was predicted in 1971 by Leon Chua, a professor of electrical engineering at the University of California, Berkeley, as the fourth fundamental device. Publishing a paper in the Nature journal by Hewlett Packard (HP) in May 2008–announced the first ever

experimental realization of the Memristor, surprised the electronics community and caused an extraordinary increased interest in this passive element. Based on the symmetry of the equations that govern the resistor, capacitor and inductor, Dr. Chua hypothesized that fourth.

Device should exist that holds a relationship between magnetic flux and charge. Since physical discovery of the Memristor, several institutions have published Memristor device fabrications using a variety of different materials and device structures Again in 2008, Stanley Williams research group in HP Lab built Memristor cross-points with engineered oxygen vacancy profiles that predictively control the switching conductance and polarity. In 2009 Biolek et al. modeled nonlinear dopant drift Memristor by SPICE One year later, WeiLu, professor at University of Michigan proposed a nanoscale Memristor device which act as synapse in neuromorphic systems Later on, In 2011 a multidisciplinary researcher from Harvard University published an interesting paper on programmable nano wire circuits for using in nano processors Memristors are promising devices for a wide range of potential applications from digital memory, logic/analog circuits, and bio-medical applications .Especially because the Memristor does not lose its state when the electrical power is turned off could be a suitable candidate for making non-volatile memrories with ultra large capacity In addition to non-volatility, Memristor has other attractive features such as simple physical structure, high-density, low-power, and unlimited endurance which make this device a proper choice for many applications. Different device structures are still being developed to determine which Memristor device would be the best option for commercial use.

This is based on many factors such as size, switching speed, power consumption, switching longevity, and CMOS compatibility.

THE THEORY OF MEMRISTORS

In 1971, Leon Chua formed the necessity for an additional essential circuit element more to the Resistor, capacitor, and inductor [4]. Chua reasoned the existence of a lacking circuit detail from symmetry reasons, gazing the six possible combos of the relationships of 4 essential circuit variables – the voltage V, current I, flux φ, and charge q, at the identical time because the rate is that the indispensable upon time of the current and therefore the flux is prime upon time of the voltage, the opposite viable relationships are connected by -terminal circuit parts. Resistors be a part of voltage to current by means that of law (V = IR), capacitors connect charge to voltage (q = CV), and inductors connect current to flux (φ = LI). The next possible relationship is that the affiliation between charge and flux and is not enclosed through any conventional circuit detail. Chua reasoned, for the sake of completeness, the lifestyles of a fourth essential circuit detail that connects the charge and flux and named the device the memristor, as a brief for 'reminiscence resistor'. The six combinations of the relationships are illustrated

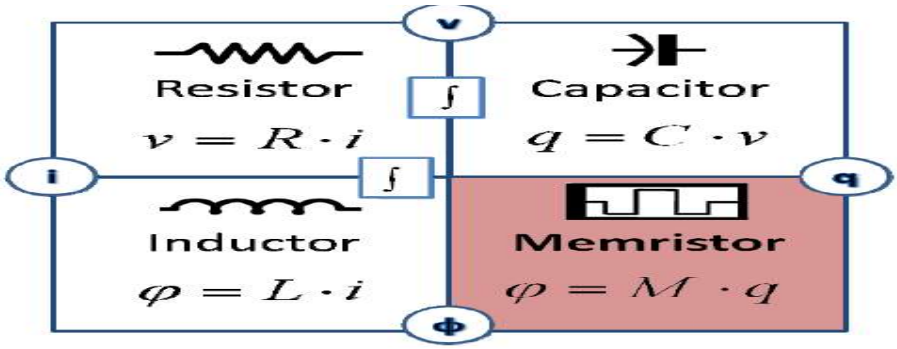


Figure Illustration of the six combinations of the relationships between voltage v, charge q, flux ϕ, and current i. The memristor connects the charge and flux.

$dwdt=fw$, ……(1)

$Vt = Rw, *i(t)$……(2)

Mq =dødq ……(3)

Where M is memristance, i(t) is memristor current, w is internal state, variable t is time

BASIC MEMRISTOR PROPERTIES

Listed below are some of the most characteristic and important features for memristors:

- Associate ac detail, dc
- No garage of electricity
- Two-point terminal circuit detail
- Pinched physical phenomenon loop among the i-v craft
- Fine or poor differential resistance
- Nonlinear q-φ curve
- Low-frequency property and frequency-established memristance; and
- Normally handiest obvious at little scales.

A number of the bullet points on this listing are typical fingerprints of memristors and should be looked for while finding out statistics from electrical measurements. Others are larger normal residences for memristors that distinguishes them from totally different constructing blocks in circuit theory. we have a tendency to shall within the subsequent see however these residences is also outlined clearly just about with support from the water analogy. We have visible however the memristance of the memristor changes with time whereas an electricity is passing via the device, indicating that it's an ac device.

MEMRISTOR BASED LOGIC CIRCUIT DESIGN

The primary consciousness here the usage of bipolar memristive device using TiO2. during this device, resistance depends upon on the trail of current flow. The polarity and image are shown:

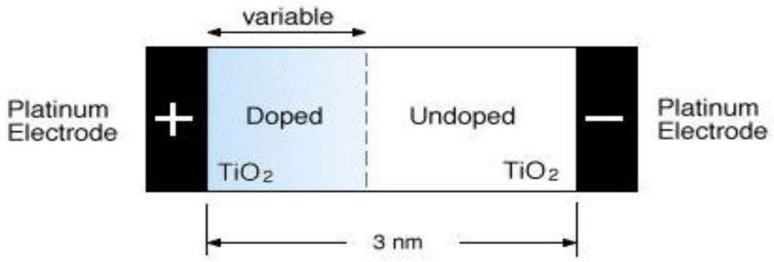


Figure 1: Memristor Device using TiO2

While current flows into the thick black line the memristance decreases, once current flows out of the thick black line the memristance will increase. There are various models like: linear particle drift model, non-linear particle float model, TEAM model. This paper makes a speciality of linear-ion flow version and additionally the TEAM model. It additionally describes the gain of team version over different models. power unit is advanced the linear particle model for the primary time to introduce memristor. The model assumes that charged ions are unfastened to maneuver below the have an effect on of big discipline, this movement changes the electrical phenomenon of the media. The integral a part of the team version is predicated whole on Associate in Nursing expression for the spinoff of the inner nation variable which will be fitted to any memristive device sort. Linear particle waft model is outlined with the help of equation: $dwdt{=}u{*}Ron{*}it.vt$ ={$Ron{*}wtD$ + $Roff$(1−wtD))*i(t)

MATHEMATICAL MODEL OF THE MEMRISTIVE CHUA'S CIRCUIT

The generalized memristor reported in [5] consists of a diode bridge with a first order parallel RC filter, as shown in Figure, whose memristive behaviour is realized using the voltage Constraints involving each pair of parallel diodes [6]. Its mathematical model is described by the following equation:

$$i = g(v_C, v)v = 2I_S e^{-\rho v_C} \sinh(\rho v)$$

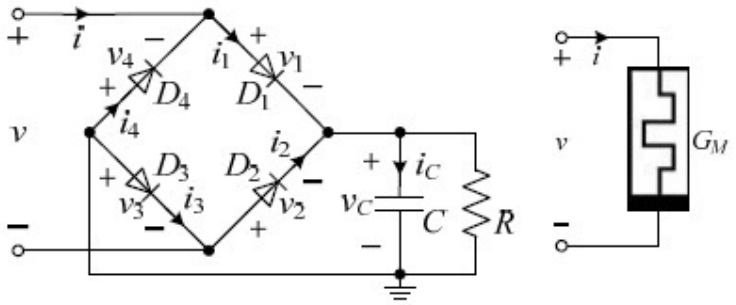
$$\frac{\mathrm{d}v_C}{\mathrm{d}t} = f(v_C, v) = \frac{2I_S e^{-\rho v_C} \cosh(\rho v)}{C} - \frac{v_C}{RC} - \frac{2I_S}{C}$$

Where ρ = 1/(2nVT), *IS*, *n*, and *VT* stand for the reverse saturation current, emission coefficient, and thermal voltage of the diode, respectively, *vC* is the state variable of the dynamic element *C*, *v* and *i* are the input voltage and the flowing current of the generalized memristor. According to Equation (1), the generalized memristor is voltage-controlled and its can be expressed by:

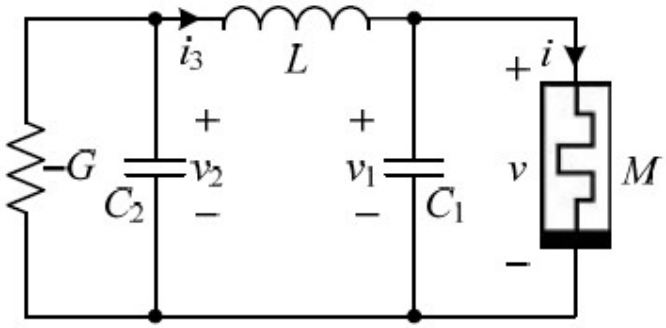
$$G_M = \frac{i}{v} = g(v_C, v) = \frac{2I_S e^{-\rho v_C} \sinh(\rho v)}{v}$$

In this circuit, *C* = 1 μF, *R* = 0.5 kΩ, and four 1N4148 diodes are used to construct the memristive diode bridge, where the diode parameters are *IS* = 2.682 nA, *n* = 1.836, and *VT* =

25 mV. When sinusoidal voltage stimuli are applied, the generalized memristor exhibits three characteristic fingerprints for identifying memristors.



Based on the topology of the canonical Chua's circuit, a memristor based chaotic circuit is established, as shown in below Figure, in which the Chua's diode is substituted by the simplified generalized memristor shown in above Figure.



With reference to Figure, there are four dynamical elements of two capacitors *C*1 and *C*2, an Inductor *L*, and the capacitor *C* inside the generalized memristor, leading to the existence of four state variables *v*1, *v*2, *i*3 and *vC*. Applying Kirchhoff's circuit laws and the constitutive relationship of the generalized memristor of the proposed circuit, we can obtain a set of first-order differential equations.

LITERATURE SURVEY

The concept of a resistor with memory existed even before Leon Chua's publication on the memristor in 1971. In 1960, Prof. Bernard widrow of Stanford University developed a new circuit element named the "memristor." The memistor was a three-terminal device for which the conductance between two of the terminals was controlled by the time-integral of the current in to the third terminal. Thus, the resistance of the memistor was controlled by charge. Memistors formed the basic components of the neural-network architecture called ADALINE (ADAAptive Linear Neuron).

In 1968, F. Argall published a paper, "Switching phenomena in titanium oxide thin films," which shows results similar to that of the memristor model proposed by Stanley Williams and his team.

In 1971, Leon Chua mathematically predicted [7] that there is a fourth fundamental circuit element characterized by a relationship between charge and flux linkage.

In 1976, Leon Chua and Sung Mo Kang published a paper entitled “Memristive devices and System” [8], generating the history of memristors and memristive systems.

In 1990, S. Thakoor, et al., [9] demonstrated a tungsten-oxide variable-resistance device that is electrically reprogrammable. It is not clear whether the memistor device described has any relation with Chua’s memristor [10].

Four years later, in 1994, Buot and Rajgopal published an article entitled “Binary information storage at zero bias in quantum-well diodes” [11]. The article described current-voltage characteristics similar to that of the memristor in AIAs/GaAs/AIAs quantum-well diodes. The analysis showed no direct connection to Chua’s memristor [10].

In 2000, Beck, et al., of IBM’s Zurich Laboratory, described reproducible resistance switching effects in thin oxide films [12]. The hysteretic features of these switches are similar to those of the memristor.

In 2001, Liu, et al., researchers in the space Vacuum Epitaxy Center of the University of Houston, presented results [13] during a non-volatile memory conference held in San Diego, California, showing the importance of oxide bi layers to achieve high-to-low resistance ratio.

In 2008, thirty-seven years after Leon Chua’s proposal, the memristor in device form was developed by Stanley Williams and his group in the information and Quantum Systems (IQS) Lab at HP. Dmitri Strukov, Gregory Snider, Duncan Stewart, and Stanley Williams, of HP Labs, published an article [14] identifying a link between the two-terminal resistance switching behaviour found in nano scale systems and Leon Chua’s memristor. The model proposed by them is described in detail in chapter 4 of this report.

Victor Erokhin and M. P. Fontana claimed to have developed a polymeric memristor [10] before the titanium-dioxide memristor developed by Stanley William’s group.

Since the announcement of the break through by Stanley William’s group, numerous papers with the aim to analyze the elementary attributes of the memristor and memristor applications in various areas of circuit design have appeared.

Later in 2008, J. Joshua Yang, Matthew D. Pickett an article [15] demonstrating the memristive switching behaviour and mechanism in nanodevices.

In January 2009, Sung Hyun Jo, Kuk-Hwan Kim, and Wei Lu of the university of Michigan published an article [16] describing an amorphous-silicon-based memristive material capable of being integrated with CMOS devices.

In June 2009, scientists at National Institute of Standard Technology (NIST) [17] reported that they had fabricated non-volatile memory using a flexbile memristor that is both inexpensive and low-power.

Mahmoud Zangenah, “Designing Energy- Efficient Sub threshold logic circuits using equalization and non-volatile memory circuits using memristors.” He depicts that memristor improves energy efficiency in sub threshold regime. It reduces energy consumptions and improves performances of digital logic circuits.

He says in the future he will explore the designing of bypass equalized flip flop that are

use in transparent mode in turn reduces setup time. Equalization techniques cloud be explore to improve the energy efficiency.

In 2010, Medha Haridas The Memristor in modern computing a computer to retain saved state while off and would requires less power [18]. Andavntage to memristor is their analog nature. Currently going on into the development of analog computers using memristors.

In 2010, R Stanley Williams proposed memristive devices which exhibit a dynamical conductance ststte that depends on the excitation history [19],can be used as non-volatile memory elements by storing informations as different conductance states. The use of the memristor is limited to the times at which power fails or its restored.

In 2010, Farnood Merrikh Bayat proposed a new and simple method for performing analog arithmetic operations. which is simpler ,require less chip area and faster than their equivalent CMOS circuits.

Farnood Merrikh Bayat, Saeed Bagheri Shourakia "Memristor Based Circuits for Basic Arithmetic Operations"

In 2011 Shahar Kvatinsky, Avinoam Kolodny and Uri C. Weiser did their work on The logic design of memristor based IMPLY (Implication) logic gate is presented .Investigating and characterizing the behaviour of memristor and IMPLY logic gate reveals several design limitations and considerations. This design procedure is the first step in the development of a general design methodology for logic based on memristors.

In 2011, Yang Liu did his research in among emerging nanotechnologies, memristors have become promosing candidates to build storage structures because of high capacity, short switching time and low power consumption. In the future, we can utilize approaches such as profiling, trace –based simulation and stastical models for evaluation to obtain more accurate results.

In 2011, Idongesit E. Ebong proposed that during memory operation, the number of read operations necessary for a write after an erase may be different [20]. This adaptive method will prevent any over erasing or overwriting. The goal of the simulation is to show the effect of current memory state on reading, erasing, and writing to a selected memristor. The energy per bit for the memristor memory compared to flash looks very promising.

In the future new methods will need to be devised that will allow for reliably writing to the device in the multibit case, as well as perform flash like operations, such as block erasures.

In 2011,Kyosun Kim, Sangho Shin proposed architecture mapped to the field programmable nanowire interconnect fabric produces a field programmable stateful logic array[21], in which general-purpose computation functions can be implemented by configuring only nonvolatile nanowire crossbar switches.

They have identified a fan-out function requirement in stateful logic for computational completeness and propose a new basic AND operation. With its inherent data-latching property, logic can effectively implement low-register-cost fully pipelined digital systems, and therefore holds potential for implementing high performance stream processors which are extensively used in consumer electronics, multimedia applications, and high-speed networking.

The architecture has been improved to achieve twice higher performance, and mapped to the FPNI fabric to yield field programmability. In this paper, novel memristive switch-based stateful logic pipeline architecture is proposed. In the future a multitude of intriguing research topics remain to be addressed for implementation of dependable FPSLAs.

In 2012, Omid Kavehei elucidated that new materials are becoming an attractive option for future memory architectures[22]. He recommends a memory array using complementary resistive switches (CRS).His approach creates the necessary design methodology platform that will assist designers in implementation of CRS devices in future systems. The CRS device shows several advantages over a single memristor element for memory applications. This research verifies that a high r(=RHRS/RLRS) does not necessarily improve the substantial amount of parasitic path currents, while a higher RLRS value guarantee a successful READ and WRITE operations. The results indicate that due to sneak-paths and leakage current, a memristive array is faced with a programming and read error rate that aggressively limit the maximum nanocrossbar array size, whereas a CRS array is less affected by these problems.

In 2012, Chul-Moon Jung proposed two new zero-sleep-leakage flip-flop circuits are proposed to make the sleep leakage literally zero[23]. The conditional storing circuit in the F-F can reduce switching power by 87% in storing the data than the F-F. We can reduce the number of transistors that should be added for the memristor retention from 15 to 8 compared to the original circuit. Some voltage generating circuits such as positive and negative charge pumps that need high voltage devices should be added to the F-F circuit. The F-F can be completely cut-off from the external power supply saving the energy leak during the sleep time.

In November 2014, Dmitry Belousov did his work on Memristors can also used for logical circuits, i.e, Memristor Aided Logic(MAGIC)[24].In each MAGIC logic gate, memristors serve as an input with previously stored data, and additional memristor serves as an output. The use of MAGIC gates within a memristive crossbar array can lead to more efficient systems in terms of performance, power consumption and to novel non-von Neuman architecture.

In 2014, Georgious papandroulidakis proposed the design of computational and reconfigurable structures that exploit unique threshold dependent switching response of single memristors and their compositions[25]. A new logic circuit design paradigm, which assumes parallel processing of input signals , along with the construction of programmable composite memristive switches of variable precision.

In 2014, Anas Mazady did his research in Modeling, Fabrication and Characterization of Memristor to reduce power consumption than CMOS circuits.

In 2015,Yang Zhang propsed memristors can be utilized as logic gates ,control switches as well as memory elements, different AND ,OR logic gates which are based on memristors [26].And also the analysis of the memristor based crossbar architecture which has a series, excellent features such as good compatibility, high density, non volatility, low power and good scalability.

In 2016, Apoorva Amdapurkar, explained Design and development of memristor based combinational circuits [27]. Memristor devices consume less power compared to CMOS.

Different circuits can be used to reject power consumption. It is highly proficient as it is combined of many digital circuits.

Area is a prominent factor which gives an excellent opportunity to realize various complex circuits in future.

In April 2018, Lin-Jie Yu produced RRAM device with layer graphite membrance and proposed a prototype model for graphane based memristor Aided Logic to implement logic operations[28].Graphite based memory device can be viable act as an alternative architecture for computation. Future study should explore the realization of more complex logic function with a simple and reliable structure.

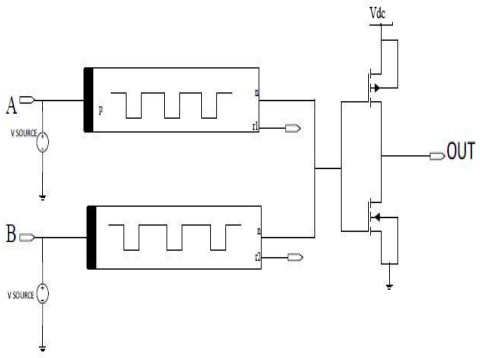
CONTRIBUTION

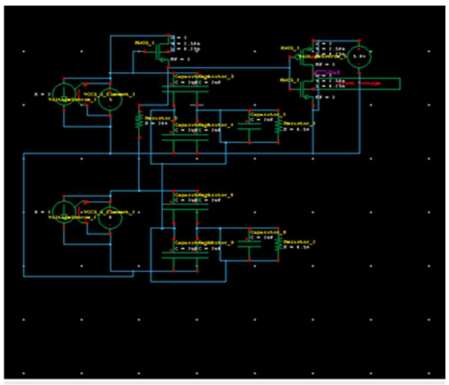
GATES DESIGN USING MEMORISTOR

This following section gives the overview of the memristive circuits implemented for the basic logic gates and its corresponding truth table.

Memristor is passive component having two terminals, and it is proficient in being equipped as a combinations of many digital circuits, storage element and logic. The main property of memristor is the data srorage. The basic two input (A and B) NAND and NOR can be implemented using memristor as shown in figure -- and figure -- respectively.The only difference between NAND and NOR is the reversed polarity. Figure--- and figure--- shows the behaviour of the NAND and NOR gate with respect to inputs (A and B).

NOR GATE

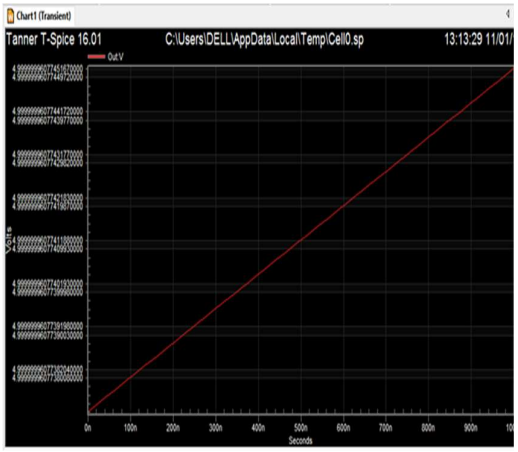


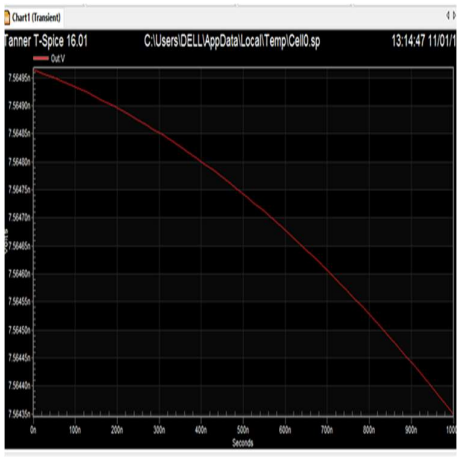


The Figure 2 shows the schematic of NOR gate using memristor.

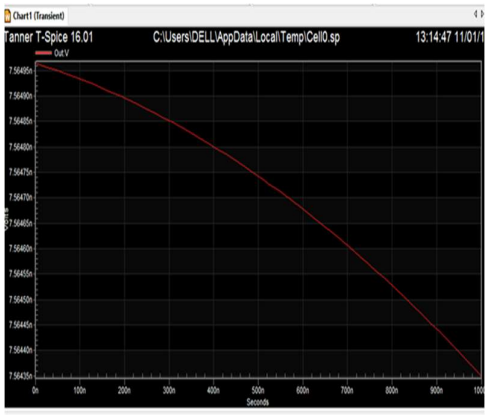
NOR gate having A and B are the inputs, so total 4 input combinations. In case of NOR gate a positive voltage source 1 (high or logic ‘1’) is applied to one input of the memristor and another input is connected to gnd(low or logic ‘0’) at the output terminal to get low voltage or logic ‘0’.

A=0 volts, B= 0 volts A=0 volts, B= 5 volts

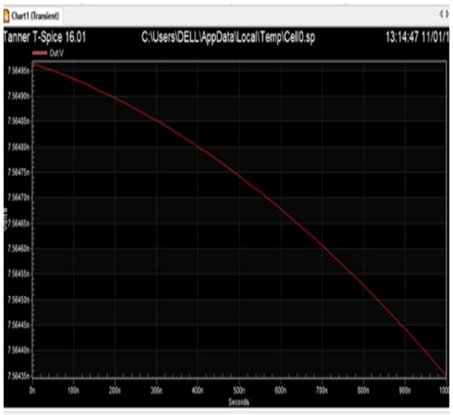




A=5 v, B= 0 v

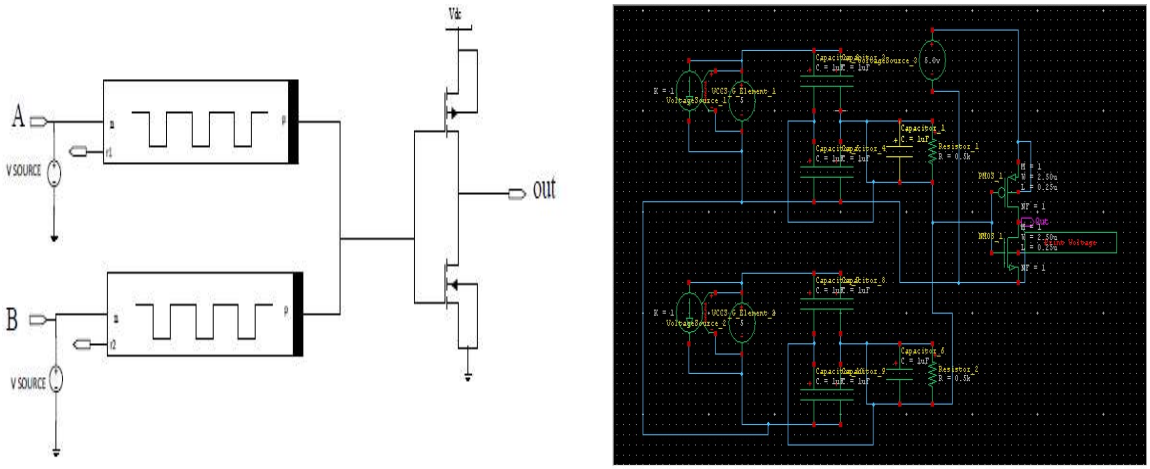


A=5 v, B= 5v



NAND GATE

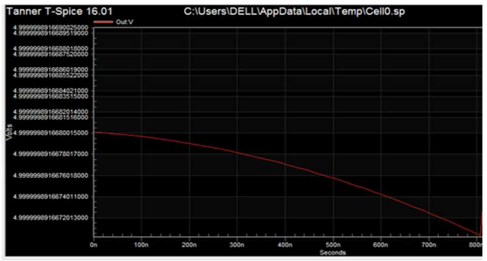
Here positive voltage supply is given to the negative terminal (n side) of the memristor which leads to shift of doping boundary (w) from n towards p.. This results in making the net resistance of the memristor equivalent to 16KΩ. Alternatively when a negative voltage supply is applied to the negative terminal of the memristor, it causes the net resistance of the memristor to decrease and it approaches to about 100Ω.



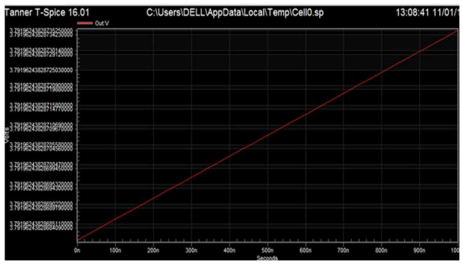
The Figure shows the schematic of NAND gate using memristor.

Similarly In case of NAND gate a positive voltage source 1 (high or logic '1') is applied to one input of the memristor and another input is connected to gnd(low or logic '0') at the output terminal to get high voltage or logic '1'.

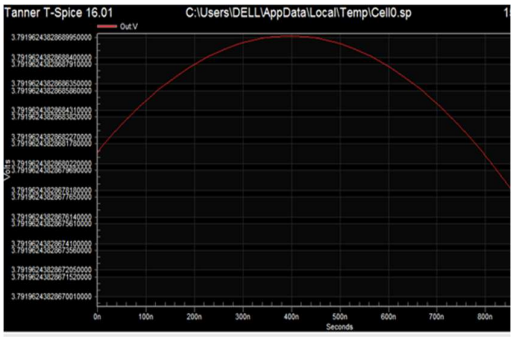
A= 0 v, B= 0 v



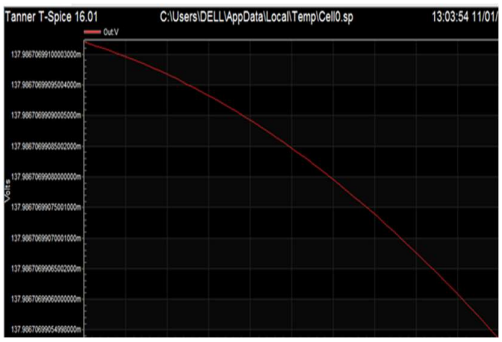
A= 0 v, B= 5 v



A= 5 v, = 0 v

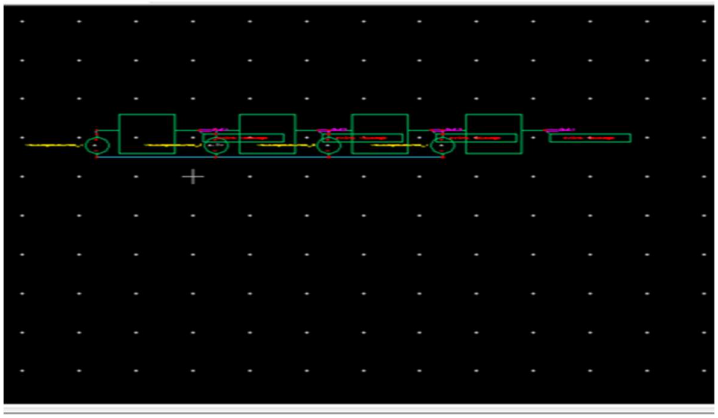


A= 5 v, B= 5 v



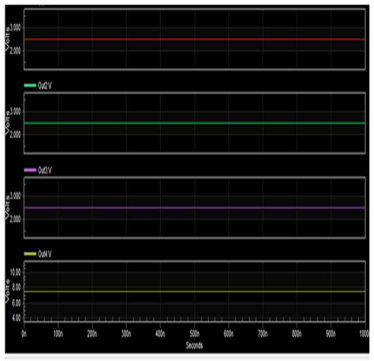
D LATCH USING MEMRISTOR

The working of D Latch using Memristor is similar to the D latch using CMOS. The A,B,C and D are the inputs,V1,V2,V3 and V4 are the outputs of 4 bit D Latch .Based on input combinations output changes its states. The D latch device having 4 inputs has 16 input possible combinations.

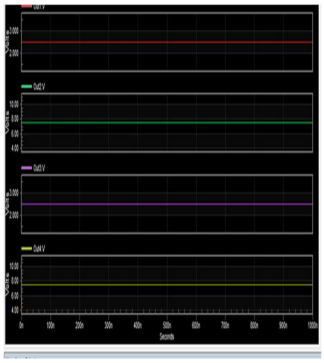


The Figure shows the schematic of D Latch using Memristor

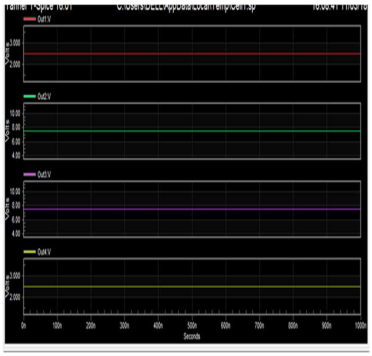
A=0v, B=0v, C=0v, D=0v



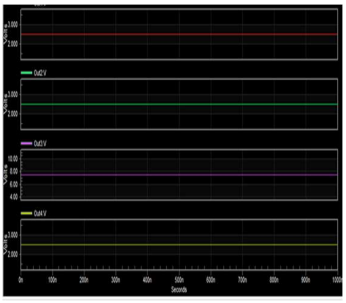
A=0v, B=0v, C=0v, D=5v



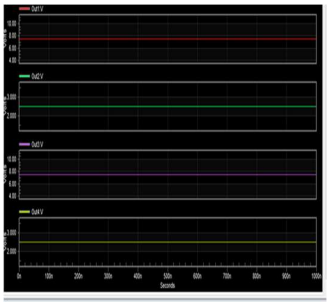
A=0v, B=0v, C=5v, D=0v



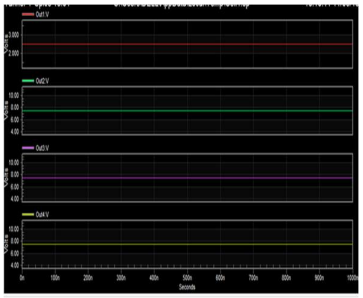
A=0v, B=0v, C=5v, D=5v



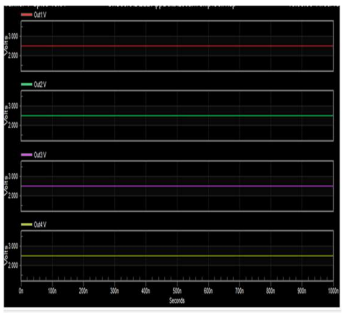
A=0v, B=5v, C=0v, D=0v



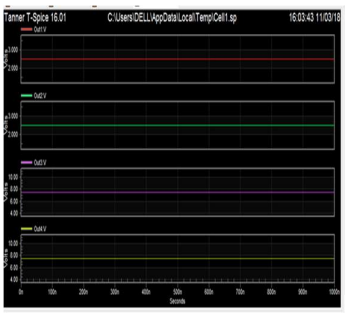
A=0v, B=5v, C=0v, D=5v



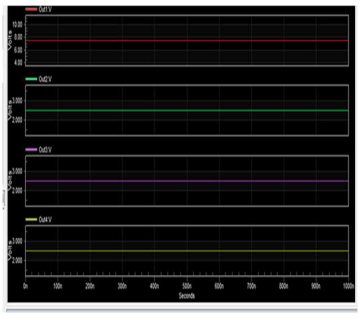
A=0v, B=5v, C=5v, D=0v



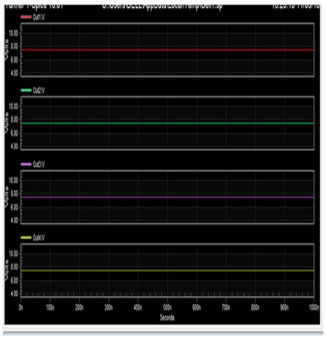
A=0v, B=5v, C=5v, D=5v



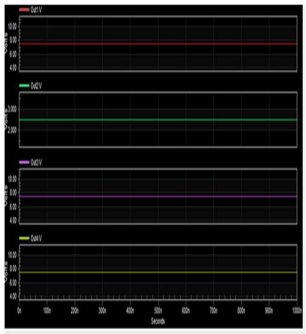
A=5v, B=0v, C=0v, D=0v



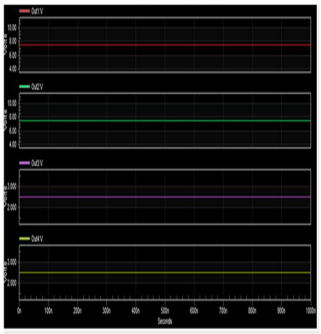
A=5v, B=0v, C=v, D=5v



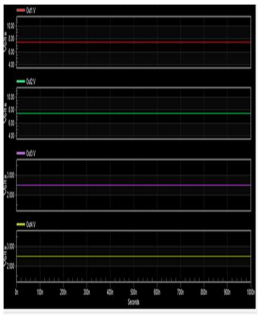
A=5v, B=0v, C=5v, D=0v



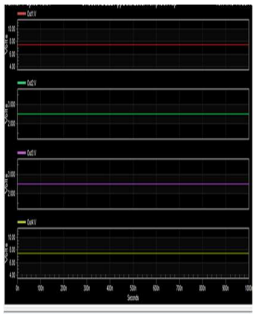
A=5v, B=0v, C=5v, D=5v



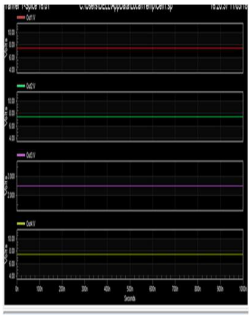
A=5v, B=5v, C=0v, D=0v



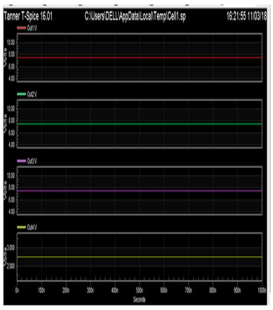
A=5v, B=5v, C=0v, D=5v



A=5v, B=5v, C=5v, D=0v



A=5v, B=5v, C=5v, D=5v



CONCLUSION

In this paper, a memristor based logical gates presented, this logic gates use comparatively less die area than that of CMOS. By using memristor NOR, NAND logic gates and D Latch, the design efforts can be reduced, power is also reduced and also transient time is reduced. Though the memristors fundamental, it still rather unknown, meaning that it is very likely that it has been very underutilized up until today. Therefore, many systems that earlier were thought to be anomalous, may actually be memristive, or memcapacitive or meminductive for that matter. Still, there remains much work to be done to implement these memory elements properly in our field.

COMPARISION

Comparision between conventional based Flip flops and Memristor based Flip Flops

S. No	Parameters	D FF(4 Bit)			NAND gate (2 Bit)			NOR gate (2 Bit)		
		Conventional	Memristor	% reduction	Conventional	Memristor	% reduction	Conventional	Memristor	% reduction
1	Power(uw)	670	240		14.40	11.52		19.5	12.6	
2	Space(um)	146.35	102.58		2.36	1.45		2.58	1.78	

3	Time(Transient Delay)(ps)	11.17	7.75		2.23	1.15		5.13	3.2	

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