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EFFECT OF THROUGH SILICON VIA THERMAL STRESS ON 3D INTEGRATED CIRCUIT RELIABILITY

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Abstract: The through silicon vias (TSVs) technology plays a significant role in 3D integrated circuits (3D ICs). TSVs have the ability to vertically facilitate enormous and short interconnects between stacked silicon dies to create 3D integrated circuits; thus, increasing their value and functionality. However, the mismatch of the coefficient thermal expansion (CTE) between the material of TSV and silicon substrates has resulted in thermal stress consequences affecting the reliability of the 3D integrated circuits containing TSVs. The aim of this systematic review is to investigate thermal stress caused by TSVs. In this review, 23 studies were selected between the years 2008 and 2022 using several inclusion and exclusion criteria. These studies were analyzed to reveal the effect of thermal stress of TSVs on the 3D IC devices, and examine some of the innovative solutions proposed in several studies to increase the performance and reliability of 3D ICs.

Keywords: 3D integrated circuits (3D ICs); through-silicon vias (TSVs); thermal stress; Annular-Trench-Isolated TSVs; polymer-clad TSVs; polymer-embedded TSVs.

1. Introduction

Over the past forty years, the development of the silicon semiconductor technology with regard to performance and productivity has greatly increased [1,2]. Moore's law has played a significant role in this development; however, the idea of minimizing transistors made this law to become no more appropriate for advancing the microelectronic industry. The semiconductor technology has the potential for producing a large-scale integration of a large number of transistors in a chip [1]. Gordon Moore postulated that "instruments of various sorts, especially the rapidly increasing numbers employing digital techniques, are starting to use integration because it cuts cost of both manufacture and design" [3].

The concept of integration especially three-dimensional (3D) integration has minimized the cost per system volume, while in the meantime increasing value and functionality. Through-silicon vias (TSVs) became the technology utilized for integration systems to facilitate 3D chip stacking [4]. Typically, 3D integrated circuits (ICs) stacking involves using vertically positioned TSVs, which are conducing material (usually copper) filled line arrays, in silicon substrates separated by an insulation layer. However, due to the mismatch between the coefficient of thermal expansion (CTE) between copper and silicon, thermal stresses are

experienced in 3D integrated circuits leading to detrimental impact on the performance and reliability of these 3D ICs [5].

1.1. Thermal Stress Of TSVs

Through-Silicon-Vias (TSVs) is a promising technology in 3D integration for their ability to vertically facilitate enormous and short interconnects between stacked silicon dies to create 3D integrated circuits and 3D packaging [6]. While TSV and 3D ICs have many advantages, thermal stress is one of the greatest challenges that may take place during the TSV fabrication process or during IC operation [7,8]. During thermal annealing, a necessary and imminent part in the 3D integration process, the degree of copper expansion exceeds that of the silicon substrate [9]. This problem arises due to the vast coefficient thermal expansion (CTE) mismatch between copper and silicon [7,8]. The CTE of copper is five times more than that of silicon and therefore, when applying a thermal load, copper was found to significantly expand much more than silicon [7,10]. This expansion contributes to specific thermomechanical TSV behavior that can potentially affect the neighboring devices [10]. This feature results in the accumulation of crack driving force and tensile hoop stress in the silicon substrate [9]. In addition, [7] reported that the thermal stress on TSVs is affected by thermal load and CTE mismatch and can be represented by the following equation:

$$\sigma_r = \sigma_\theta = \frac{-\mathrm{E}\,(\alpha_{tsv} - \alpha_{si})\,T_{tsv}}{2 - 2_v},\ \sigma_Z = 2\sigma_\theta \quad (1)$$

Where σ_r is the radial stress, σ_θ is the circumferential stress, and σ_Z is the axial stress. The CTE of TSVs is represented by α_{tsv}, α_{si} is the CTE of silicon, and the T_{tsv} is the thermal load on TSV. The thermal load is the difference between room temperature and TSV temperature. Moreover, E is the Young's modulus, and υ is Poisson's ratio. The thermal load of TSV is the only variable after identifying the type of metal and diameter of the TSV and when all other parameters are constant. Thermal stress ca be reduced by minimizing TSV thermal load [7].

1.2. Effect of Thermal Stress

Thermal stress has a great impact on the performance and reliability of the structure of 3D integrated circuits. Thermal stress has a bad effect on the IC structure by increasing the TSV keep out zone (KOZ), and causing cracks in copper and silicon substrate, destruction of dielectric materials, copper protrusion, interfacial delamination, and performance deterioration leading to reliability concerns and failure in the TSV structure [7,8,10]. The protrusion of copper in TSVs was found to cause damages to the BEOL structure [10].

Table 1. Comparison of the CTE of Several Materials

Material	CTE (ppm/°C)
Copper	17.7
PBO	35-55
BCB	42
Si_3N_4	3.2
SiO_2	0.51
Silicon	3.05
Tungsten	4.6

In a study by [11], thermal stress was simulated by exposing the 3D structure to a thermal change from 250 °C to 25 °C and analyzed to examine its effect on carrier mobility and the mechanical reliability of the 3D structures. To achieve this purpose, a finite element method (FEM) 3D simulator was utilized [11]. The results of this study proved that thermal stress has the ability to influence and change carrier mobility in p- and n-silicon TSV and this change is affected by the geometry and material of TSV. The coefficient of thermal expansion (CTE) mismatch was found to change with the type of material. Table (1) shows different types of materials used in 3D integrated circuits and their CTEs. The TSV thermal stress can cause cracks that jeopardize the reliability of the 3D structure [11].

There are several techniques for measuring stress for TSV reliability such as micro-Raman spectroscopy, and x-ray diffraction (XRD) [10]. Micro-Raman spectroscopy is a well-known method used for measuring the near-surface silicon stress surrounding through silicon vias [10,12]. In a study by [13], x-ray microscopy along with deep learning detection workflow were used to analyze stress and describe delamination defects.

1.3. Innovative Ways for Overcoming Thermal Stress

Due to the damaging effect of thermal stress, several innovative ideas were depicted in literature that can assist in minimizing TSV stress and optimize power performance [10]. It was widely depicted that the isolation liner has a critical role in determining the effectiveness of the TSV performance. That is because the properties of the liner such as its thickness and dielectric constant play a key role in the TSV capacitance (C_{TSV}). $C_{TSV} \propto \varepsilon/d$, where ($\varepsilon$) and (d) are the dielectric constant and liner thickness respectively [14]. The TSV and Si substrate act as a parasitic capacitance regarding their high polar character [15]. The smaller C_{TSV} the lower power loss, latency, and cross talk [14]. Recently, polymer liners have caught the attention as a replacement for SiO_2 for their adequate properties and easy processing and they can be applied by spin coating [10,14].

Polymer liners were shown to have no polar character; thus, they can reduce capacitance and contribute to less TSV stress [10,15]. One of the polymers mentioned in literature is Benzocyclobutene (BCB) which was applied by [16] using it with a thickness of 5 μm for a TSV of a 30 μm diameter. The results revealed that BCB can reduce stress along the interfaces of Cu/BCB and BCB/Si [16]. The same result was obtained by [15] when BCB was spin coated at 600 rpm and cured for one hour at 250 °C. Spin coating was effective when used with TSV with scallop resulting in a flat TSV surface [15]. In the studies of [15,17] the polymer of polybenzoxazole (PBO) was introduced and found to reduce the capacitance modulation. Both BCB and PBO can contribute to high TSV and 3D ICs performance and reliability [15].

In this paper, a systematic review was conducted to examine and analyze research studies that address thermal stress of TSVs, its impact in the reliability of the 3D ICs and some of the innovative solutions for this phenomenon that are proposed in literature. A systematic review is defined by Cook et al. as “the application of scientific strategies that limit bias by the systematic assembly, critical evaluation and synthesis of all relevant studies on a specific topic” [18]. This systematic literature review focuses on the thermal stress, a drawback for using through silicon vias in the 3D integrated circuits. For this purpose, research studies from the last 15 years were collected and extensively reviewed to find the suitable articles for the topic discussed. Different databases were utilized to find articles that analyze thermal stress and its

distribution and characteristics, as well as that propose innovative methods to address thermal stress effects. All collected articles were analyzed and evaluated to address the problem of thermal stress resulting from TSVs and affecting the 3D integrated circuits as a whole.

The aim of this systematic review is to comprehend the diversity of approaches regarding the effect of thermal stress on the reliability of TSVs in the context of 3D ICs, guided by the recommendations of [19] for conducting a systematic literature review. Moreover, issues such as the factors used to analyze thermal stress, experimental methods and simulations used to understand and measure it, and solutions and innovations to overcome the problem were employed to investigate selected studies. Section 2 includes the research method used to finish this systematic review. Section 3 introduces the results of this review along with the discussion and section 4 includes the conclusion.

2. Research Method

The methodology strategy for this systematic literature review is based on selecting literature and using knowledge related to the thermal effect of TSV on 3D ICs, methods to have better understanding about this problem and what possible solutions can be applied. Studies pertaining to this area of research have been investigated and analyzed using the guidelines from [19] and research questions were developed. These questions are used as the first step in the search process followed by choosing databases and suitable key terms to be used to find relevant papers that address the topic of this review [19,20]. All papers resulting from the initial search were subject to inclusion and exclusion criteria to extract primary studies. This search was then refined to select the more relevant studies to the thermal stress of TSV. This is followed by collecting data from selected studies and analyzing and documenting the results and discussion. This systematic review is meant to introduce existing knowledge regarding a specific area of research from studies available in the literature to fill the gap in research and reinforce the field of study [21].

2.1. Research Questions

The research questions, formulated for this systematic review, are designed to help in extracting all data from literature that concerns thermal stress in TSV, factors that affect this stress, and possible methods for reducing this complex problem in 3D ICs. Thermal stress is an obstacle in TSV fabrication and needs to be investigated and analyzed. The research questions for this review are:

RQ1. What is the knowledge provided in literature concerning thermal stress caused by TSV and its effect on the performance and reliability of 3D ICs?
RQ2. What are the proposed solutions available in the literature to increase the performance and reliability of 3D ICs?

This systematic literature review provided the answers of these research questions for those researchers and decision-makers who seek literature to better understand the thermal stress of TSV, its impact on the performance of the whole system used, and new ways to have more reliable systems.

2.2. Search String

The process used to detect and examine trusted databases in literature was based on automatic search. To complete this search, it was mandatory to find effective key terms. Key terms such as “through silicon vias” or “TSV”, “thermal stress,” and “3D integrated circuits” or “3D ICs” were employed. Boolean operators were used with the key terms to search different academic databases [19]. The search form is: “thermal stress” AND (“Through silicon vias” OR “TSV”) AND (“3D Integrated Circuits” OR “3D ICs”). This form was used in four databases: IEEE Xplore, SpringerLink, ScienceDirect, and Google Scholar to find journal articles and conference proceedings and papers that were published between the years 2008 and 2022. Various databases allowed obtaining all studies relevant to the chosen topic on thermal stress of TSV in 3D ICs. The search was based on only choosing studies in the English language. The result of the initial search and databases used are depicted in Table (2).

Table 2. Initial Search and Electronic Databases

Electronic Databases	Initial Search
IEEE Xplore	148
SpringerLink	2097
ScienceDirect	459
Google Scholar	11,100
Total Number of Initial Search	13,804

2.3. Inclusion and Exclusion Criteria

After the initial search, the total number of studies collected from all electronic databases used reached 13,804, which is too large. However, more refinement is needed using the inclusion and exclusion criteria based on the recommendations in [19]. A manual search was conducted to find the more relevant studies on the topic from all the papers included in the initial search. The inclusion criteria for this manual approach were based on: choosing reliable primary studies that are full text, relating directly to thermal stress of TSV in 3D ICs, including experimental methods, and can effectively answer the research questions.

The exclusion criteria were based on excluding all duplicates, secondary studies, and studies that do not address thermal stress related to through silicon via in 3D ICs. The eligibility criteria are illustrated in Table (3). The process of the inclusion and exclusion criteria is executed by reviewing the titles, abstracts and conclusions of all initially selected studies to review their relevance to the researched topic, then a more thorough inspection is performed to review the full text of the studies that their abstracts and conclusions seemed irrelevant, before deciding to exclude them.

Table 3. Eligibility Criteria

Inclusion Criteria	Exclusion Criteria
1. Reliable primary studies 2. Full text 3. Relating directly to thermal stress of TSV in 3D	1. Duplicates 2. Secondary studies 3. Do not address thermal stress related to through silicon via in

ICs 4. Including experimental methods 5. Can effectively answer the research questions	3D ICs.

3. Results and Discussion

The results of this systematic review are divided into several parts to address the outcomes of the search and selection approach and the outcomes of analyzing the contents of the research studies.

3.1. Search Results

The search was conducted to find the adequate and most relevant studies to the research topic and that can answer the research question. Therefore, the initial search that include the four databases: IEEE Xplore, SpringerLink, ScienceDirect, and Google Scholar. As previously illustrated, the total number of studies collected from the initial search was 13,804 from all databases. These studies were divided into 148 from IEEE Xplore, 2097 from SpringerLink, 459 from ScienceDirect, and 11,100 from Google Scholar.

The collected studies were published in the last 15 years and in the English language. However, these studies were subject to the inclusion and exclusion criteria including only the most relevant studies to the topic discussed - thermal stress of TSV in 3D ICS, that were primary sources, and can answer the proposed research questions. The primary studies after removing secondary papers were 9,265 and after including only full text were 6,479. All irrelevant studies were excluded leading to including 383 studies. Moreover, all duplicates were excluded from this systematic review leading to including only 48 studies. The strategy used to apply the inclusion and exclusion criteria and come up with the most relevant studies was based on inspecting the titles, abstracts and conclusions and then reviewing the full text before deciding what studies to exclude in the final search. The outcome of the final search included 23 studies that were analyzed in this review.

Moreover, the 23 selected studies were analyzed on the bases of year of publication. Figure (1) illustrates the changes in the number of studies published per year on the thermal stress of through silicon vias in 3D ICs during the selected period. Figure (1) shows that thermal stress of TSVs was studies in most of the years discussed except for the years 2008, 2010, and 2020, which show no real contributions in this area of research. The number of publications fluctuates through the years; however, the year 2012 included the most published studies (4 studies), followed by the years 2018 and 2022, where there are 3 published studies in each of these years, and then there are 2 published studies in each of the years 2009, 2011, 2016, and 2017. In addition, the first study in the selected period was published in May 2009 in the 59th Electronic Components and Technology Conference in San Diego, California.

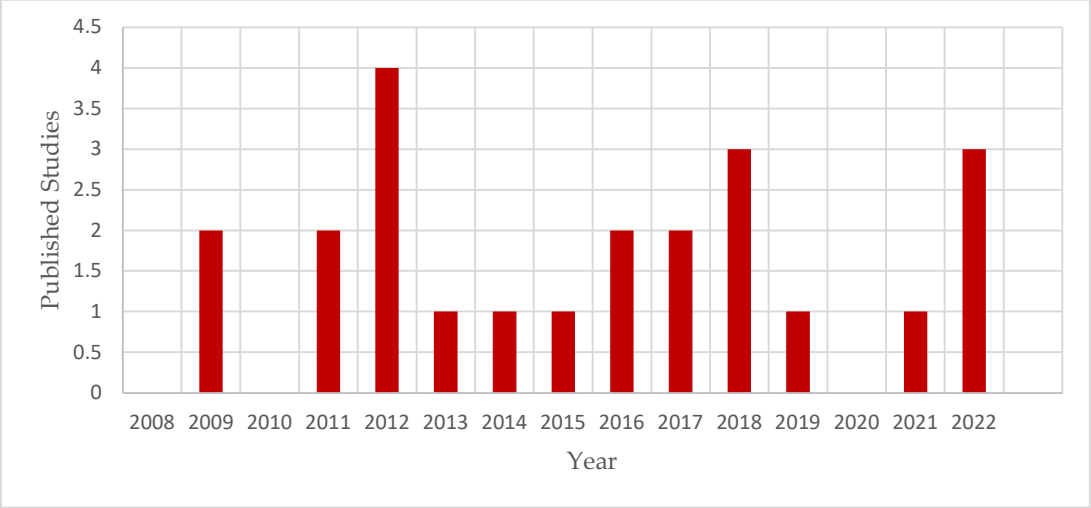

Figure 1. Published studies by year.

Furthermore, Figure (2) includes the number of studies arranged by the type of journal or conference used.

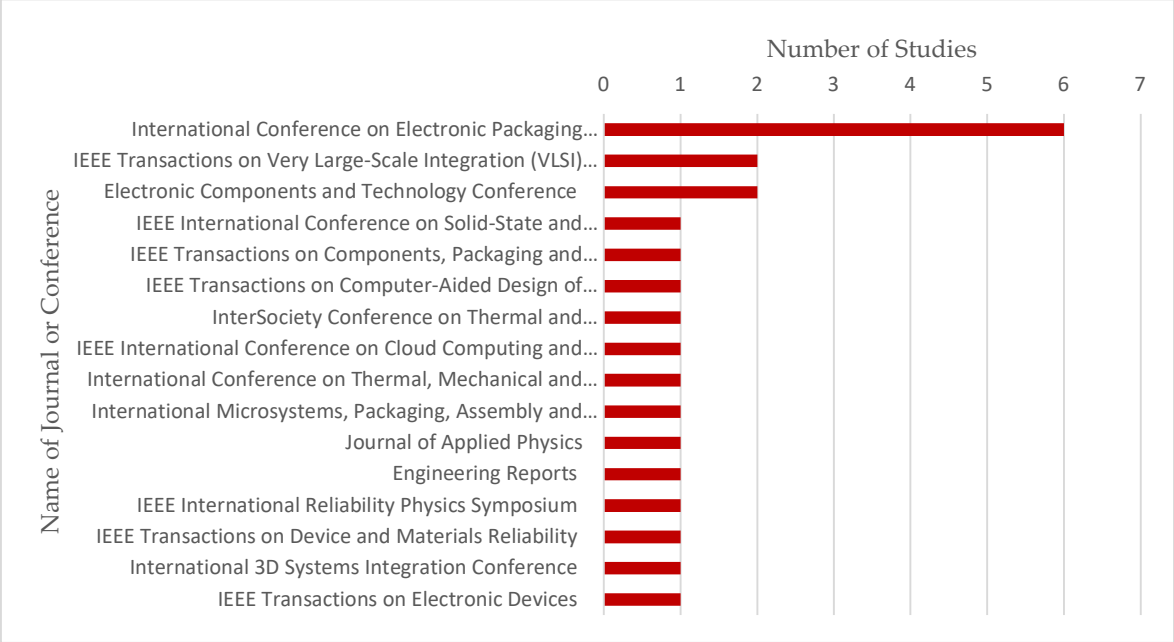

Figure 2. Studies per journal or conference

As illustrated in Figure (2), the top three journals included more than one published article. The *International Conference on Electronic Packaging Technology is on top of all publishers that has 6 published studies on thermal stress of TSV in 3D ICs. Moreover, each of the journal of IEEE Transactions on Very Large-Scale Integration (VLSI) Systems and the* Electronic Components and Technology Conference included 2 published studies. However, each of the other 13 journals and conferences that were used in this study contributed to only one published study on the topic. It is no surprise that most journals and conferences were technology oriented. In this systematic review, 7 journals and 9 conferences were utilized, indicating the

significance of the impact thermal stress on the usability and reliability of 3D integrated circuits.

There are several factors that were addressed in the selected studies to discuss thermal stress, analyze it, and measure it. All these issues are illustrated in Table (4) along with the articles that discuss them. For example, one of the factors discussed in most articles are the TSV dimensions such as diameter, pitch, and thickness. TSV dimensions are discussed in the studies of [9,10,11,16,22,23,24,25,26,27,28,29,30,31,32,33]. Other factors for measuring thermal stress include in-plane stresses such as the radial stress and the circumferential stress that were discussed in [13,22]. Temperature variations are used to measure thermal stress in [10,34]. It was found by [34] that the stress value increases both when the temperature in high and low; however, this value was the smallest at room temperature. Moreover, other factors such as TSV materials in [11], Cu microstructure in [10], thermal conductivity in [7], location of defects in [27], wall delamination defects in [13,16], crack driving force in [9], and the size of the keep-out-zone (KOZ) in [29] were discussed to analyze and measure thermal stress.

Table 4. Factors For Measuring Thermal Stress

Factors for measuring Thermal Stress	Sources
TSV dimensions	[9], [10], [11], [16], [22], [23], [24], [25], [26], [27], [28], [29],
In-plane stresses	[30], [31], [32], [33]
Temperature variations	[13], [22]
Copper microstructure	[10], [34]
Die thickness	[10]
Thermal conductivity	[7], [35], [37]
Line configuration on crack driving force	[7]
	[9]
TSV materials	[11]
Wall delamination defects	[13], [16]
Location of defects	[27]
Keep-out zone (KOZ) size	[29]

To achieve the measurement and analysis of thermal stress, several experimental methods and simulations were used to understand thermal stress as depicted in table (5). The finite element analysis (FEA) was the most employed analytical and simulation model used in most studies [9,11,16,22,24,25,26,27,28,30,31,32,33,35,36,37,38]. Other measuring models were used such as the Raman spectroscopy in [10,22,31,34], the precision wafer curvature technique in [22], bending beam technique in [10], indentation in [10], design time & run time in [7], 3D x-ray microscopy (XRM) in [10,13], deep learning object detection workflow in [13], ANSYS multi-physics simulation platform in [24], knowledge-oriented nonuniform (KONU) refinement strategy in [36], RBF neural network algorithm in [33], the design of experiments (DOE) in [38], and other analytical approaches in [9,16,29].

Table 5. Experimental Methods & Simulations

Experimental methods & Simulations	Sources
Raman spectroscopy	[10], [22], [31], [34]
Precision wafer curvature technique	[22]
Finite element analysis (FEA)	[9], [11], [16], [22], [24], [25], [26], [27], [28], [30], [31], [32], [33], [35],
Bending beam technique	[36], [37], [38]
Indentation	[10]
Design time & run time	[10]
3D x-ray microscopy (XRM)	[7]
Deep learning object detection	[10], [13]
workflow	[13]
Analytical approach	[9], [16], [29]
ANSYS multi-physics simulation	[24]
platform	[36]
Knowledge-oriented nonuniform	
(KONU) refinement strategy	[33]
RBF neural network algorithm	[38]
Design of experiments (DOE)	

There are different negative consequences associated with TSV thermal stress that are mentioned in the selected studies and illustrated in table (6).

Table 6. Effects of Thermal Stress

Effects of Thermal Stress	Sources
Increasing keep-out zone	[10], [22], [27]. [28]
(KOZ)	[7], [9], [10], [11], [13], [16], [26],
Si cracking	[28], [29], [30], [35]
	[7], [10], [11], [13], [16], [28], [30],
Interfacial delamination	[35]
Via extrusion	[13]
Degradation of Cu liner	[13]
Degradation of TSV structures	[13], [23], [26], [31], [33]
Reduction of carrier mobility	[27], [32], [36]

Silicon cracking and interfacial delamination are the most mentioned consequences. Silicon cracking is discussed in the studies of [7,9,10,11,13,16,26,27,29,30,35]. The generated thermal expansion forces, resulting from the TSV thermal stress, that work in opposite directions have the ability to cause fatigue in the stacked chips leading to the thinning of silicon substrate and cracking [7]. Moreover, interfacial delamination was discussed in [7,10,11,13,16,28,30,35] and increasing of keep-out zone (KOZ) was discussed in [10,22,27,28]. Other consequences included via extrusion and degradation of Cu liner in [13], degradation of TSV structures in [13,23,26,31,33], and reducing carrier mobility in [27,32,36].

As shown in table (7), some of the innovations and solutions to overcome the problem of thermal stress due to TSV in 3D ICs. Some studies introduced new ways such as using polymer-enhanced TSVs to reduce thermal stress due to TSV and electrical loss as in [10]. Polymer-enhanced TSV included polymer-clad TSVs have the ability to reduce TSV stress and liner capacitance and polymer-embedded TSVs can enhance electrical performance [10].

Table 7. Innovative Solutions

Innovative Solutions	Sources
Polymer-enhanced TSVs	[10]
Polymer-clad TSVs	[10]
2-stage thermal management methodology: Design-time & run-time	[7] [31], [35]
Annular-Trench-Isolated TSV (ATI TSV)	[23], [29] [23]
BCB to replace the SiO2 insulating layer	
Parylene layer to replace the SiO2 insulating layer	

A 2-stage thermal management methodology: design-time & run-time was used as in [7] to reduce the thermal challenges on the integrated circuit architectures. Annular-Trench-Isolated TSV (ATI TSV) was used in [31,35] for its simple fabrication process and cost. The ATI TSV can minimize thermal stress in silicon substrate through focusing the stress in the copper/silicon interface inside TSV and that is why it can used as an innovative solution for 3D IC integration with stress sensitive devices [31,35]. The BCB to replace the SiO2 insulating layer were used in [23,29], and Parylene layer to replace the SiO2 insulating layer were used in [23]. Both benzocyclobutene (BCB) in [23,29], and Parylene in [23], were found to effectively reduce thermal stress for TSV structure.

4. Conclusion

This systematic review paper introduces the studies published between 2008 and 2022 about thermal stress of the TSV structure and its effect on the reliability and performance of the 3D integrated circuits. Despite the significant role of TSV in the development of the technology of integrated circuits, there are some drawbacks associated with thermal stress due to CTE. This review presents 23 studies that discuss thermal stress and use a variety of experimental methods and simulations to measure it. Some of these studies proposed innovative solutions to reduce thermal stress and increase the performance and reliability of 3D ICs such as using polymers and annular-Trench-Isolated TSV (ATI TSV).

Based on the literature, there was no systematic review about thermal stress of TSV that has been published in the period discussed. Accordingly, this review provides the basis for future research on thermal stress. Future work can focus on new approaches and other innovative solutions to enhance the reliability of 3D integrated circuits by reducing TSV thermal stress in more cost-effective ways.

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