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DESIGN OF GDI BASED FIR FILTER FOR ECG SIGNAL FILTERATION

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Abstract:
Improvements in IC technology have continuously lowered component sizes over the last several years, forcing the inclusion of additional operational circuits on each chip. Novel GDI technique circuitry has been the center of attraction in the development of digital circuits owing to its lower power consumption and efficient use of resources. GDI technique contain less number of transistors and a maximum speed for efficiency and reliability. This article analyzes the implementation of a Finite Impulse-Response (FIR) filter using GDI technique and fundamental blocks like adders and multipliers. In this research, a GDI-FIR filter is designed for ECG signal filtering. The simulation findings show that proposed FIR filter design using GDI logic reduces power consumption and improves performance.

1. Introduction

Many academic scholars have concentrated on the design of low-power VLSI systems with the goal of providing a variety of mobile telecommunications and computation technologies in the present day. With the advancement of VLSI circuits, low-power mobile devices have recently been designed and produced for a number of applications. In most cases, the prerequisites for low power utilisation should be satisfied with the equally challenging objectives of high device density and throughput. The weight as well as dimensions of the battery impact the overall size of the system. In truth, battery technology has usually trailed behind advancements in device and circuit technology. These limits have created a number of challenges for designers working on VLSI circuits in low-power solutions. This has fuelled greater research into circuits with high speed, high throughput, small chip area, and low power. Moore's law states that "the number of transistors in a tiny integrated circuit roughly doubles every two years." ." Nonetheless, the progress of IC advancements in technology has exceeded Moore's law. This 100-fold increase in flash storage chip capacity over the previous eight years exemplifies Moore's law's predicted exponential proliferation of integrated technology. This remarkable progress has caused a shift in mobile devices, with flash storage now acting as the dominant storage media [1,2].

The bulk of signal-processing algorithms would be built on the addition operation. For high-performance DSP systems that employ a finite impulse response (FIR) filter, the low-power adder is crucial. As a consequence, increasing adder speed in all modules is crucial. As

a consequence, constructing a low-power adder has become a critical component of creating a low-power VLSI design. The adder architecture has also been designed to improve its speed and throughput rates, which are expected to affect the efficacy of DSP algorithms in the forthcoming decades. Because of the increasing proliferation of mobile communications and other portable device technologies, power consumption is a major design concern. At various levels of system design, including circuit, device, and architectural levels, power-saving methods have been devised. The far more challenging aspect is preserving the functionalities while aiming to reduce power consumption. At different phases of design, the researchers focused on the design of adders to reduce power consumption[3,4].

2. Design of FIR Filter for ECG Signal Processing

ECG signal monitoring and control entails three key responsibilities: ECG signal processing and quantization, as well as wireless transmission. The QRS complex is perhaps the most important element of an ECG. The characterization of a QRS complex wave is the most integral feature of ECG signal analysis and interpretation.The accuracy of the QRS complex wave detection is essential to the effectiveness of all ECG detection techniques. . The literature has several ways for detecting QRS complexes. To construct the QRS complex diagnosis in addition to compressing the ECG signal data, the bi-orthogonal wavelet transform dependent technique is used. The development of a low power FIR filter has been employed to develop an effective wavelet transform technique.

The employment of decimator as well as undecimator configurations with a FIR filter is required for biorthogonal wavelet transform. In this transformation method, the ECG signal has been filtrated filtering to produce subbands . After filtering, 50% of the data is rejected using the Nyquist criterion. When implemented, such filters result in less computational burden due to the reduced number of coefficients. On the contrary, cascaded filtration decreases hardware complexity and circuit power usage. The design of the suggested wavelet filter bank is shown in Figure 1. With in the proposed wavelet filter bank design, the ECG signal is typically channeled first via a triggering sequence of filters. By designing the filters as FIR types, the system's hardware cost and power consumption may be reduced even more[5,6].

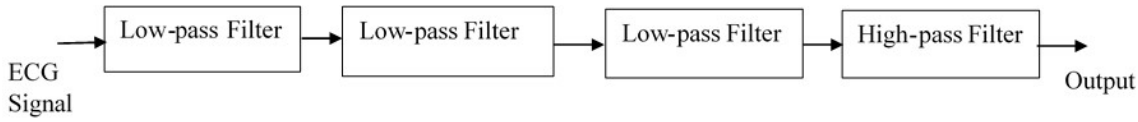

Figure 1: Block Diagram of Filter Bank in Wavelet transformation

The essential graphical depiction of the N-length FIR filter configuration is shown in Figure 2. Due to the delay, computations on the prior input signal may be done. Because the h(n) values suggest the multiplicands, the result for time n might be the total of the previous delayed samples multiplied by the relevant coefficients. x (n) represent the input sample sequence, h (n) represents the filter coefficients, and m represents the number of taps. Each register has a one-unit sampling delay. To produce the outcome, the delayed inputs were combined using wavelet coefficients. FIR filters are frequently designed entirely employing digital components.

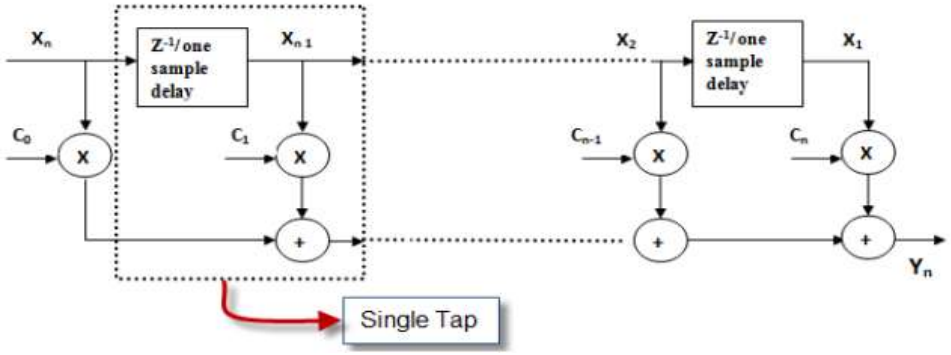

Figure 2: Direct form FIR Filter

The following formulas might hypothetically represent a FIR Filter. The core concept of the FIR filter would be a series of multiplications followed by addition. Consider the equation to demonstrate the functioning of an FIR filter:

$$y[n] = x[n] * h[n] \quad \ldots\ldots\ldots\ldots 1$$

x- input signal , y- output signal , h- transfer function. The formulation of a FIR filter is

$$y[n] = \sum_{i=0}^{i=M} b_i x[n-i] = \sum_{i=0}^{i=M} h[i] x[n-i] \quad \ldots\ldots 2$$

2.1 Implementation using GDI logic

The proposed concept simply includes the creation of a low power FIR filter. Additionally, by integrating low-pass filters with FIR types, computing cost and power utilization of the proposed architecture might be reduced still further[7,8]. The function generator of LPF is obtained using Eqn. .3.

$$H(z) = 0.125 + 0.375z^{-1} + 0.375z^{-2} + 0.125z^{-3} \quad \ldots\ldots\ldots\ldots 3$$

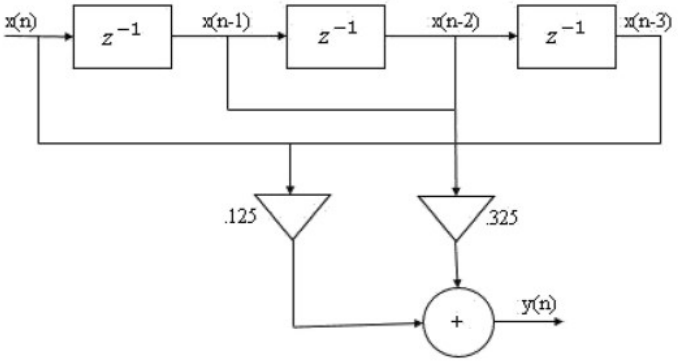

Figure 3: Block Diagram of Low-Pass FIR Filter

2.2 Design of 1-bit HTL Full Adder

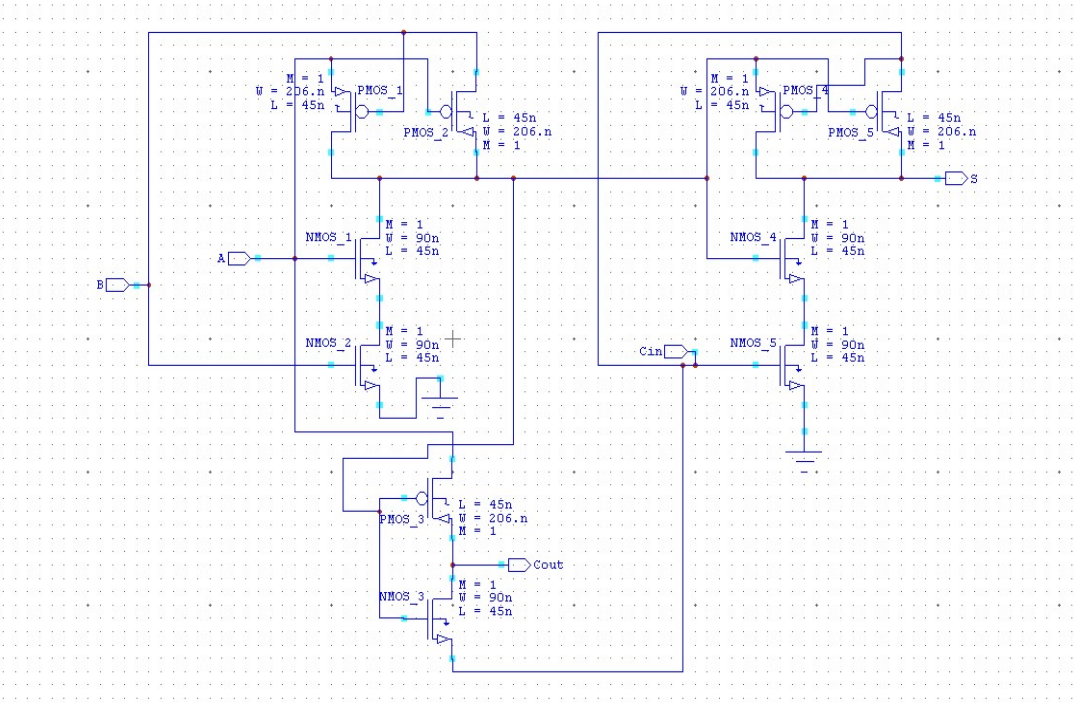

Figure 4: Schematic of 10-T HTL Adder

Since the GDI technique allows for the implementation of advanced logic gates with only two transistors, the GDI dependent 1-bit adder circuit shown in Fig. 4 requires only ten transistors. In the circuit, there are currently two blocks. The second one is a carry block, whereas the initial one is a summation block. The circuitry employs two XOR gates as well as a mux. This Sum block is implemented with two XOR gates. This gate has an A XOR B output and accepts two inputs (A, B). The output was sent to the next XOR gate, which includes an additional input C and four MOSFETs. The XOR gate provides the Sum block output as A XOR B XOR C. (S). The carry block selection circuit is made up of two MOSFETs. The choosing line of the carry block is really the result of the first XOR gate, meaning that the carry block outcome (COUT) is possibly determined by "A XOR B." The carry block output is "A" when "A XOR B" = "0." COUT symbolises "C" if "A XOR B" equals "1." The Mux circuit is formed by the transistors PMOS3 and NMOS3, while the two XOR gates are formed by the transistors NMOS1, NMOS2, PMOS1, PMOS2, and NMOS4, NMOS5, PMOS4, PMOS5.

2.3 **D-Latch:**

A unit sample delay would be employed in conjunction with D-Latch. Because the filter is often built with linear phases, a new design idea for an eight-tap filter includes just 4 coefficients and 4 bits for every coefficient. Each memory cell consisted up of a D-Flip-Flop and then 8-bit register is built. The DFF circuit using GDI is shown in Figure 5. [9,10].

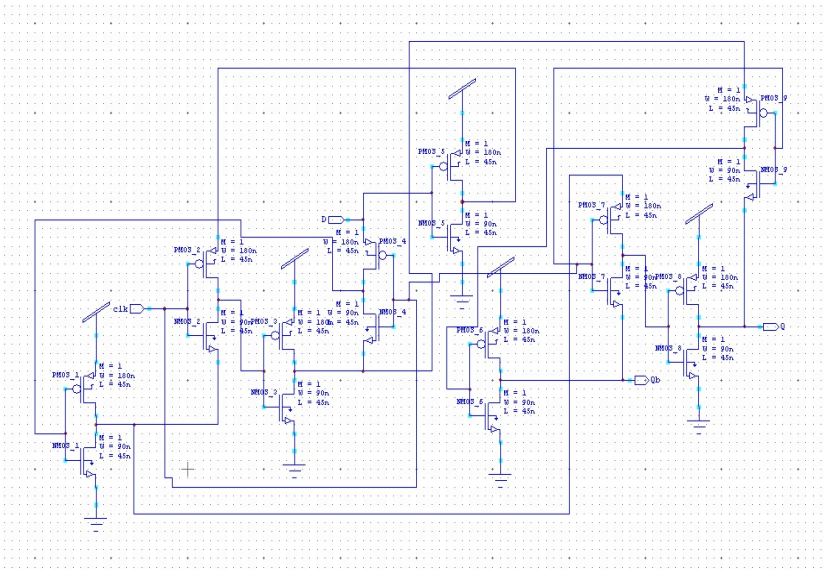

Figure 5: Schematic of GDI Logic based D-Latch

5.4 Multiplier

In the present design, a 4-bit array multiplier is used as shown in Figure 6. Implementation of multiplier is made simpler by the hardware architecture for array multiplication's one-to-one hierarchical connection with manual multiplication. There are other more capable functional multiplier designs because of its simplicity [11-13].

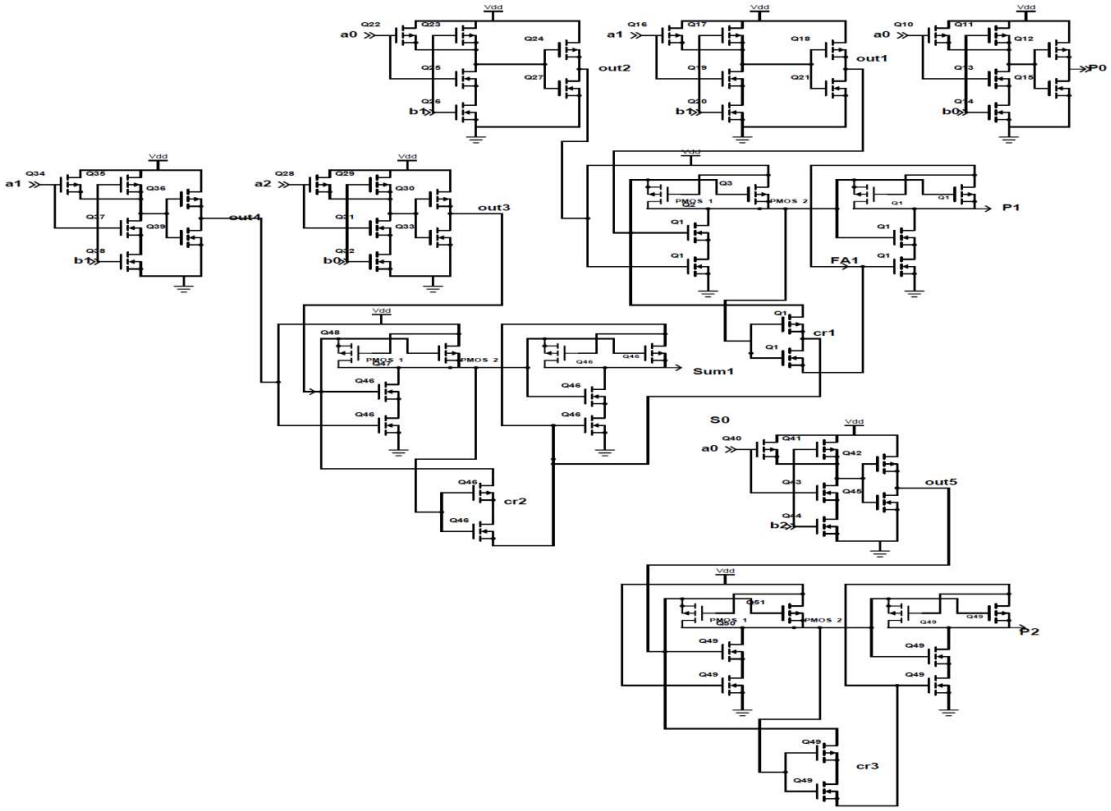

Figure 6: Schematic of 2-Bit Array multiplier

By incorporating the unit adder, multiplier and delay samples in equation 3, an FIR filter using

GDI logic is implemented as shown in Figure 7.

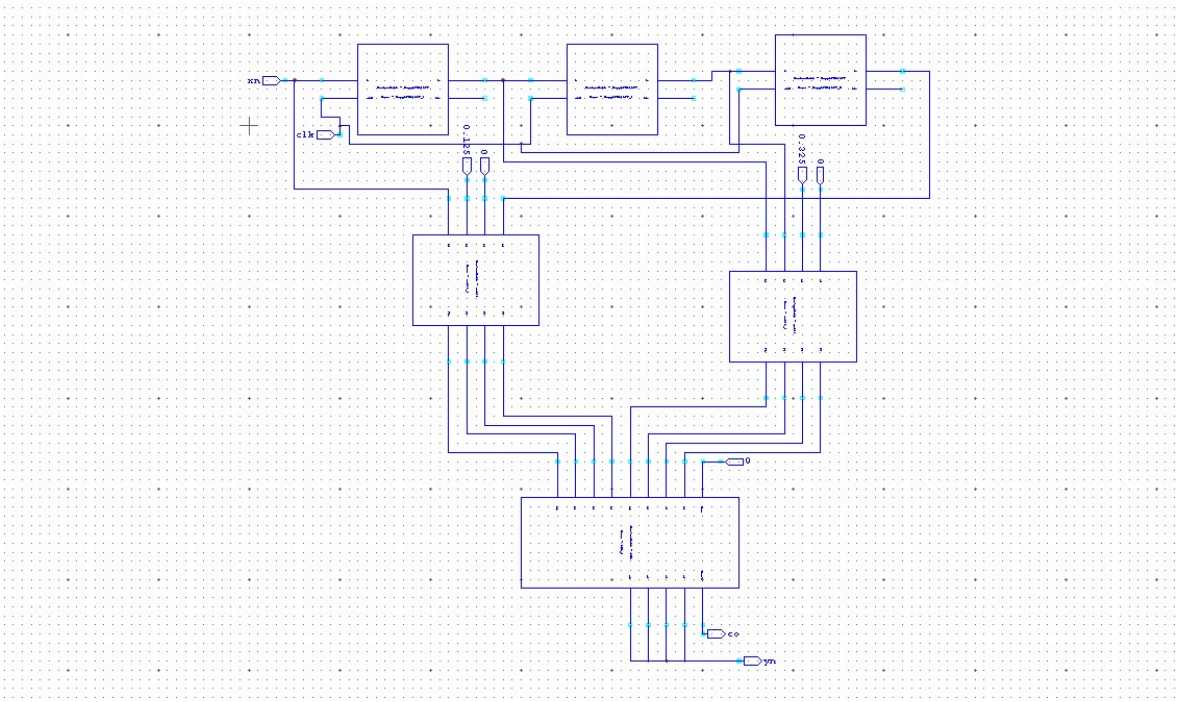

Figure 7: Design of FIR filter in GDI logic

3. Simulation Results

To assess the effectiveness of the FIR filter, a GDI technique-based HTL adder and multiplier have been developed and conducted in Tanner EDA tools employing CMOS 45nm technology. In the analytical evaluation, performance parameters such as power usage, delay, and number of transistors are considered. To ensure consistency in comparisons, the FIR filter circuit specified in the findings is done at a frequency of 20 kHz at a temp of 27°C. In this investigation, the ratio of W and L values given to each transistor utilising GDI technology was replicated using the ratio equal to 2.21. Figure 8 demonstrates the observed outcomes of a GDI technique FIR filter. As a result, we shall contrast the performance in this section with other simulated outcomes. The simulation is run using delay, power, and supply voltages of 0.8 V. According to the data, the suggested FIR filter outperformed in terms of both power and PDP. According to Table 1, the overall delay of the suggested filter is decreased by 30% when compared to the traditional filter. The average power of the proposed filter utilising hybrid transistor logic multiplier is 97% lower than that of the current FIR filter using CMOS multiplier.

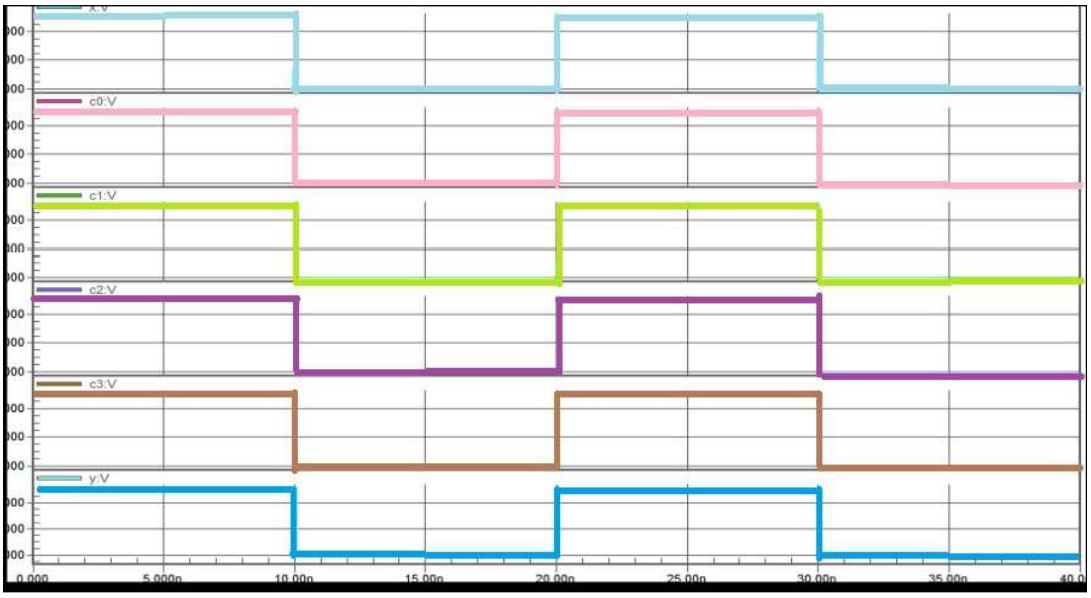

Figure 8: Transient analysis results of FIR Filter

Table 1 Performance Comparison of FIR Filters

	Delay (ns)	**Power (mW)**	**PDP pJ**
Conventional Filter[12]	108.92	27	2940.84
Proposed Filter	79.58	1.07	85.15

4. SUMMARY

The FIR filter architecture is created, constructed, and then evaluated in Tanner EDA tools to determine power usage and latency. Simulation findings show that the GDI-based FIR filter offers the best power and delay when compared to others. Compared to a typical filter employing a CMOS multiplier, the proposed filter utilises a hybrid transistor logic multiplier that minimises the number of transistors. When compared to the conventional filter, the proposed filter has a 30% lower total latency. When compared to the present FIR filter utilising CMOS multiplier, the average power of the suggested filter using hybrid transistor logic multiplier is reduced by 97%. Based on the results, it is clear that the proposed hybrid multiplier-based FIR filter might be used in bio-medical applications.

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