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DEFECTS DETECTION IN INTEGRATED CIRCUITS WITH DESIGNFOR TEST BY USING SCAN INSERTION APPROACH

V.Ashok Kumar[1], K. Mounika[2], K.Krishnamraju[3], Chaitanyakumar Marpu[4], Sanapala umamaheswararao[5]

[1]Professor at Department of E.C.E, Aditya Institute of Technology andManagement, Tekkali, India.

[2]M.Tech scholar at Department of E.C.E, Aditya Institute of Technology and Management, Tekkali, India.

[3,4,5]Assistant Professor , Department of E.C.E, Aditya Institute of Technologyand Management, Tekkali, India.

Abstract

Smaller feature size increases manufacturability Defects in ICs lead to bad chips. A very small flaw can easily lead to one. If the feature size is less than 100nm, there is a problemwith the transistor or bond wires. Moreover, it only takes one defective transistor or wire to make an entire chip fail. To function properly or at the required operating frequency. However, there were also shortcomings Due to unavoidable manufacturing processes, there is a high possibility of IC failure. Therefore, whether the product is a VLSI device or an electronic device, testing is necessary to ensure a defect-free product. A system consisting of many VLSI devices. You also needto test your component at various stages during the manufacturing process. Here, DFT is used to identify defect sites within the chip using additional designs added to the chip. Making chips testable makes it easier to find faulty chips in the field. To address this issue, we use "scan insertion" during synthesis. In this paper, we use Mentor graphics –Tessent tool to perform the proposed scan insertion

Keywords: Feature size, DFT (Design For Test), Scan Insertion, Defect

I-Introduction:

With intensity of combinational logic increases then the testability of chip is decreasing. The difficulty of achieving adequate testability of sequential circuits isamore serious problem. Given the large number of internal states, it may take many input events to bring the sequential circuit tothe desired internal state. Furthermore, determining the exact internal state of a sequential circuit from its main output may require lengthy verification experiments. Asa result, a conscious design for testability (DFT) approach requires a more structured approach to testing designs that contain a lotof sequential logic. It is difficult to view the responses captured at the primary outputs oflarge sequential (non-scanned) circuits and adjust the values Of the flops across the primary inputs. To fix this, use "Scan Insertion" during synthesis Problems, user- excluded. The term for this is non-scan flop.Figure 1 shows an example of

inserting observation points into a logic circuit with three nodes with low observability.

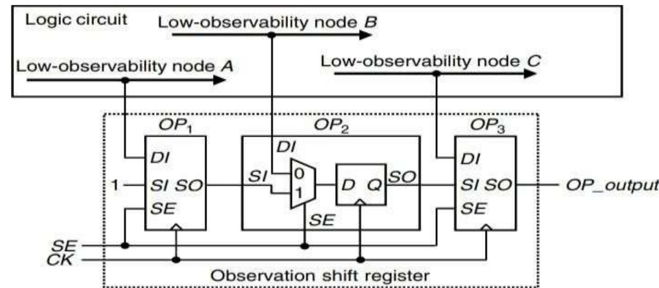


Figure-1: Observation point insertion.

II-Scan Insertion:

By inserting scans, you can also control the inputs of various gates and flip-flops in the chip, and observe the outputs of internal flip- flops according to a schedule. Replaces all selected flops with scan flops. By setting the input pins to the appropriate values, the chip first enters a special "scan mode" mode. Connect each scan cell with a scan chain.One of the primary input pins feeds the input of the first flop in that chain in scan mode. The result of the last flop is carried over to the primary output.

Figure-2.1: Scan Chain formation.

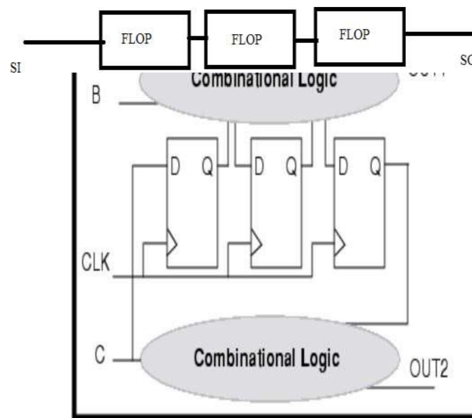


Figure-2.2: Before Scan

The design portrays in Figure 2-2 contains both combinatorial and sequential parts. Before adding scan, the design had three inputs, A, B, and C, and two outputs, OUT1 and OUT2. This "pre-scan" version is difficult to initialize to a known state, makingit difficult **both** to control the internal circuitry and **to** observe its behavior at the design's key inputs and outputs.

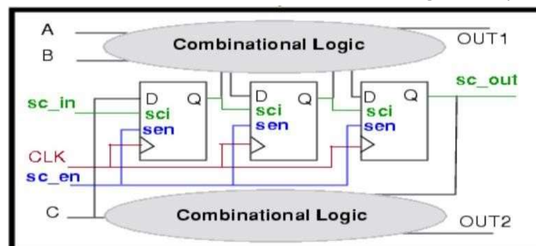
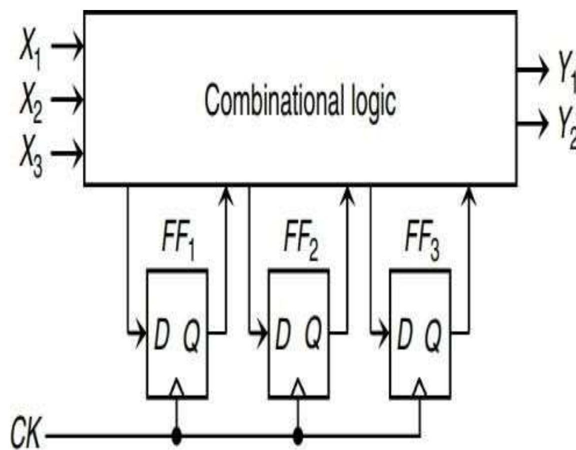


Figure-2.3: After Scan

After adding **the** scan **circuit,** thedesign **will have** two additional inputs, sc_in and sc_en, and one output, sc_out. **A scan** memory **element replaces** theoriginal memory **element,** so when **shift** is enabled **(sc_en** line is active), scan data is read from the sc_in line.

III-Scan architectures:

The scan architectonics are as follows: i) a full-scan design in this case combinational Automatic test pattern production is utilized for test generation and all flip-flops elements are turned into scan cells; ii) partial-scan design, in this case, sequential Automatic test pattern production is customarily utilized for test generation and a subset of flop elements are tuned into scan cells; (iii) A random- access scan design will use a random addressing mechanism as a substitute serial scan chains to allocate direct read and write access to any scan cell. All flop components in a full scan design are reset by the scan cellsand converted into shift registers



(also called scan chains) duringshift operations. Therefore, it is convenient to manage all combinational logic inputs in combination with those controlled by scan cells and monitor all combinational logic outputs including those controlled by scan cells. The main advantage of full-scan design is that it redirects the cumbersome problem of continuous automatic test pattern generation to the simpler problem of combinatorial automatic test pattern generation. A form of the full-scan design known as the "just about full-scan design" does not substitute scan cells for all of the flops components. These flop elements are excluded from the scan design for functional reasons, such as flop elements controlled by external clock domains that are considered overly complex, or for performance reasons, such as flop components on key paths. Sequential circuits,often using 3D flip-flops**,** are sketched in Figure 3.1. Figure 3.2 shows an equivalent multiplexed D full scan circuit. Three multiplexed-D cells S-flip-flop1, S-flip-flop2**,** and S-flip-flop3 are associated with three D-type flip-flops, flip-flop1, flip-flop2**,** and flop3**.** Automatic test pattern creation**.** The no-frills problem of combinatorial automatic test pattern generation. A form of full-scan design knownas "fast full-scan design" does not replace all flop components with scan cells. These flop elements are excluded from the scan design for functional reasons, such as flop elements controlled by external clock domains that are considered overly complex, or for performance reasons, such as flop components on keyroutes. Sequential circuits using 3D flip- flops are often sketched in Figure 3.1. Figure shows an equivalent multiplexed D full scan circuit. Three multiplexed D-sensecells S flip-flop1, S flip-flop2**,** and S flip- flop3 are

associated with three D-type flip-flops, flip-flop1, flip-flop2, and flip-flop3. We will replace it.

Figure 3.1 Sequential circuit example.

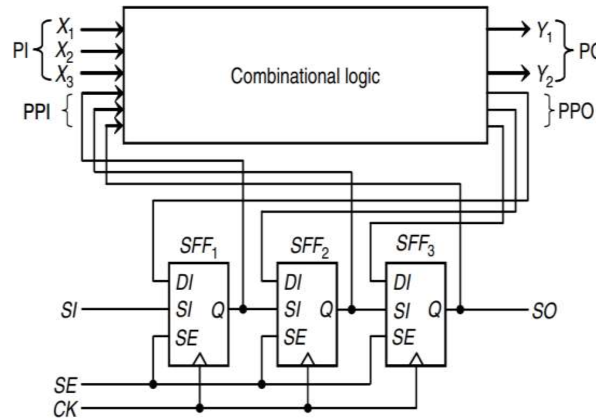


Figure 3.2 test operations.

IV -Design rules for Scan:

A design be compelled by a set of scan designspecifications in place to incorporate scan towards it. A distinct set of design approaches must also be kept away becausethey may keep under control the degree of fault coverage that may be carried off. In order to successfully use scan and fulfill thetarget fault coverage goal, a number of scandesign principles are obligatory, which are listed in Table 4.1. Each specimen of a scandesign rule violation is listed in this table along with a potential fix. All shift and capture procedures must fix scan design rules that are marked as "avoid." Avoid during shift scan design rules should be changed in course of the shift operation. A few mandate scan design guidelines are given in-depth descriptions.

Table 4.1 Typical Scan Design Rules

Design Style	Scan Design Rule	Recommended Solution
Tristate buses	Avoid during shift	Fix bus contention during shift
Bidirectional I/O ports	Avoid during shift	Force to input or output mode during shift
Gated clocks (muxed-D full-scan)	Avoid during shift	Enable clocks during shift
Derived clocks (muxed-D full-scan)	Avoid	Bypass clocks
Combinational feedback loops	Avoid	Break the loops
Asynchronous set/reset signals	Avoid	Use external pins
Clocks driving data	Avoid	Block clocks to the data portion
Floating buses	Avoid	Add bus keepers
Floating inputs	Not recommended	Tie to V_{DD} or ground
Cross-coupled NAND/NOR gates	Not recommended	Use standard cells
Non-scan storage elements	Not recommended for full-scan design	Initialize to known states, bypass, or make transparent

Bus confliction happens when 2 bus drivers push tristate buses with opposing logic values,

which can harm the chip. Bus confliction is not intended to occur during normal operation and is often avoided incourse of the capture operation because cutting-edge automatic test pattern algorithms can generate test patterns that ensure only one bus driver is in charge of a bus. However, such assurances cannot beprovided while doing the shift operation; consequently, each tristate bus must undergosome modifications to ensure that only one driver is in charge of the vehicle. In additionto bus confliction, a bus without a pull-up, pull-down, or bus keeper may result in fault coverage loss. The cause is that testing for a stuck-at-1 error at a bus driver's enable signal is challenging since the value of afloating bus is uncertain. A pull-up, pull- down, or buskeeper can be added to address this issue. One solution to this issue is the bus keeper added in, which compels the bus to retain thelogic value steered into it beforethe bus becomes buoyant. A common designstrategyfor diminishing the power utilizationis clock gating, which eradicates the pointless flop element switching activity. Figure 4.1 portrays an illustration. At the CK rising edge, the clock enable signal (EN)is created. At the clock failing edge, the clock enable signal is put into the latch LAT. Next, the flip-flop DFF's timing is turned on or off using CEN. Clock gating is a valid strategy to reduce power consumption, but it prevents some flip-flop clock ports from being driven directly from their primary inputs. Therefore, an adjustment **is** requiredto perform scan shift operations on these flop elements.

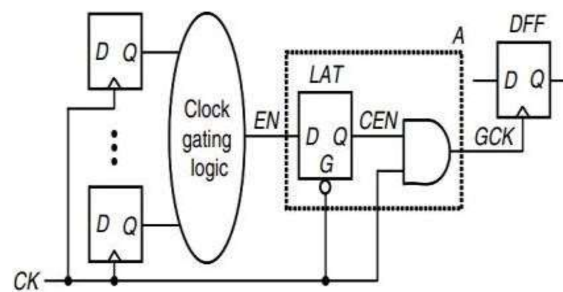


Figure -4.1 Original circuit.

An internal clock signal, such as one produced bya phase-clinched loop, frequency divider, or pulseproducer, is referred to as a procured clock. These clock signals should be ignored throughout the testing process for testing logic fed by the source clock, as the extracted clocks cannot be immediately managed by the primary inputs**.**

Combinational feedback loops can add oscillatory or sequential behavior into a design be subjected to in case the number of inversions is even or odd. This can bring about an expansion in test creating intricacy or a decrease in shortcoming inclusion on the grounds that the worth put away in the know can't be not entirely settled during testing. The best answer for this issue is to change the RTL code that creates the circle, as Combinational criticism circles are not a proposed plan practice. Asynchronous set/reset signals from scan cells that are not directly controlled by primary inputs can impede data shifting in scan chains. These asynchronous set/reset signals must be pushed into an inactive state during the shiftoperation in order to get around this issue. Itis common to refer to these asynchronous set/reset signals as being sequentially managed.

V- Scan design flow:

Despite the fact that scan design is conceptually straightforward, carefulplanning is required to incorporate scan in a way that makes it a scan design. This frequently calls for numerous circuit acclimations, all of which must be carried carefully to preserve the circuit's regular operation. Additionally, in order to ensure that scan testing can be carried out properly, numerous physical implementation elementsmust be considered. Last but not least, athorough grasp of scan design is mandatory in place to a cut above plan ahead on which scan design criteria must be followed and which debug and diagnose features must be incorporated to enable simulation, debug, andproblem prognosis. The two crucial scanprocesses of shift and capture are where caution must be used to ensure that the scan design can function properly. All scandesigns must be created so that the shift operation operates correctly regardless of whether there is clock skew between different clock domains or within the same clock domain. All scan designs share thesame capture operation, albeit some scan designs have stricter scan design guidelines than others. It must be planned so that the created test patterns' expected answers may be accurately and deterministically predicted by the ATPG tool. Basic knowledge of the applied logic simulation and fault models isrequired for this. Figure 5.1 depicts a typicaldesign process for including scan in a sequential circuit. In this illustration, pre synthesis RTL designs or post synthesis gate- level designs are first subjected to scan design rule inspection andrectification. is known as a netlist. A testable design is the finished product of the scan repair process. The testable design is transformed into a scandesign using scan synthesis when all scan design rule violations have been found and fixed. One or more scan chains are now included in the scan design for scan testing. For ATPG,a sweep extraction stage is used to remove the last output engineering of the output binds and to additionally approve the trustworthiness of the output chains. In order to ensure that the awaited responses obtained by the zero-delay simulatorutilized in test production or fault simulation match the full- timing behavior of the circuit under test, scan Finally, verification is carried out for both capture and shift operations.

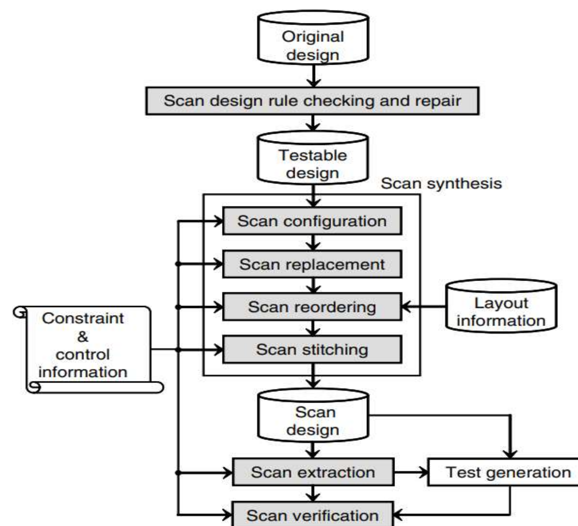


Figure-5.1 Typical scan design flow.

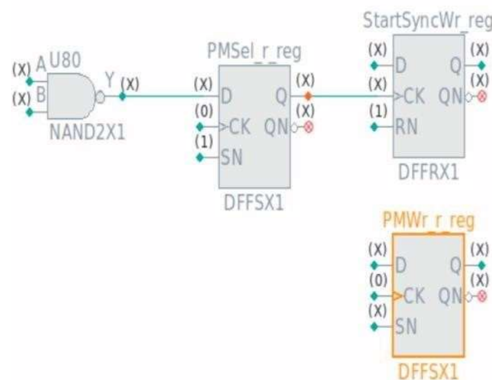
VI- Results :

```
module DmaWr ( DmaOut, PmaOut, PMSel, PMWr, DMSel, DMWr, IACKbarOut, IncCr,
    PmdIn, DmdIn, CountWr_r, FastClk, Reset, ISbar, IWrbar, IADIn,
    IDMACrOut, PMAccGnt, DMAccGnt, St34, St56, IDMACrInLat, IDMACrWrLat,
    IALIn, IDMACrWrCore, CountRd_r );
  output [13:0] DmaOut;
  output [13:0] PmaOut;
  output [23:0] PmdIn;
  output [15:0] DmdIn;
  output [1:0] CountWr_r;
  input [15:0] IADIn;
  input [15:0] IDMACrOut;
  input [15:0] IDMACrInLat;
  input [1:0] CountRd_r;
  input  FastClk, Reset, ISbar, IWrbar, PMAccGnt, DMAccGnt, St34, St56,
     IDMACrWrLat, IALIn, IDMACrWrCore;
  output PMSel, PMWr, DMSel, DMWr, IACKbarOut, IncCr;
  wire   n290, StartWr, N43, N44, MemWrSync1, N49, LoadWrbuffer, PMSel_r,
     DMSel_r, PMWr_r, DMWr_r, n77, n90, n91, n92, n93, n103, n109, n125,
     n126, n127, n128, n129, n130, n131, n132, n133, n134, n135, n136,
     n137, n138, n139, n140, n141, n142, n143, n144, n145, n146, n147,
     n148, n151, n154, n155, net207063, net207064, net207065, net207057,
```

Figure-6.1 : The sample netlist forwhichscan insertion is done.

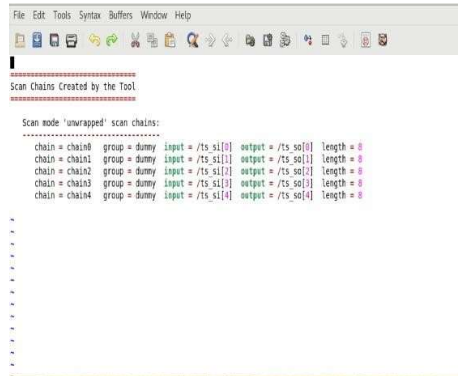
Figre-6.2 S1-violation: from MentorGraphics output

The figure-6.2 shows the drc violation that isclock is not controllable from top port. So controllability and observability is lost.



Figre-6.3 S1-violation: MentorGraphics outputs

The figure-6.3 shows the drc violation that is clock and set and reset are not controllable from top port. So, controllability and observability is lost.



The figure-6.4 Scan chain formation after scan insertion: from Mentor Graphics

```
Scan mode 'unwrapped' scan cells:
----------------------------------------------------------------------------------------------
        Chain   Group                                  ShiftReg   Library              Clock    Clock
CellNo  Name    Name   Pathname                        ID/CellNo  ModelName  ScanOut   Pinname  Polarity
----------------------------------------------------------------------------------------------
-       chain0  dummy  /ts_lockup_latchn_clkc1_intno9_i   -/-     TLATNX4              FastClk  (-)
0       chain0  dummy  /IDmaWrbufOut_reg_5_               -/-     SDFFQX1    Q         FastClk  (+)
1       chain0  dummy  /IDmaWrbufOut_reg_6_               -/-     SDFFQX1    Q         FastClk  (+)
2       chain0  dummy  /IDmaWrbufOut_reg_7_               -/-     SDFFQX1    Q         FastClk  (+)
3       chain0  dummy  /PMSel_r_reg                       -/-     SDFFSX1    Q         FastClk  (+)
4       chain0  dummy  /CountWr_r_reg_0_                  -/-     SDFFRX4    Q         FastClk  (+)
5       chain0  dummy  /CurrentState_reg_1_               -/-     SDFFRX4    Q         FastClk  (+)
6       chain0  dummy  /CurrentState_reg_2_               -/-     SDFFRX4    Q         FastClk  (+)
7       chain0  dummy  /DMSel_r_reg                       -/-     SDFFSX4    Q         FastClk  (+)
-       chain1  dummy  /ts_lockup_latchn_clkc2_intno17_i  -/-     TLATNX4              FastClk  (-)
0       chain1  dummy  /IDmaWrbufOut_reg_21_              -/-     SDFFQX1    Q         FastClk  (+)
1       chain1  dummy  /IDmaWrbufOut_reg_22_              -/-     SDFFQX1    Q         FastClk  (+)
2       chain1  dummy  /IDmaWrbufOut_reg_23_              -/-     SDFFQX1    Q         FastClk  (+)
3       chain1  dummy  /IDmaWrbufOut_reg_0_               -/-     SDFFQX1    Q         FastClk  (+)
4       chain1  dummy  /IDmaWrbufOut_reg_1_               -/-     SDFFQX1    Q         FastClk  (+)
5       chain1  dummy  /IDmaWrbufOut_reg_2_               -/-     SDFFQX1    Q         FastClk  (+)
6       chain1  dummy  /IDmaWrbufOut_reg_3_               -/-     SDFFQX1    Q         FastClk  (+)
7       chain1  dummy  /IDmaWrbufOut_reg_4_               -/-     SDFFQX1    Q         FastClk  (+)
-       chain2  dummy  /ts_lockup_latchn_clkc3_intno25_i  -/-     TLATNX4              FastClk  (-)
0       chain2  dummy  /IDmaWrbufOut_reg_13_              -/-     SDFFQX1    Q         FastClk  (+)
1       chain2  dummy  /IDmaWrbufOut_reg_14_              -/-     SDFFQX1    Q         FastClk  (+)
2       chain2  dummy  /IDmaWrbufOut_reg_15_              -/-     SDFFQX1    Q         FastClk  (+)
3       chain2  dummy  /IDmaWrbufOut_reg_16_              -/-     SDFFQX1    Q         FastClk  (+)
4       chain2  dummy  /IDmaWrbufOut_reg_17_              -/-     SDFFQX1    Q         FastClk  (+)
"scan_cells.rpt" 52L, 5385C                                                  1,1          Top
```

The figure-6.5 Scan cell report after scaninsertion: from Mentor Graphics

VII- Conclusion:

The identification of defects in the fabricated chip is very crucial and the method of scan insertion and subsequent methods of scan compression and automatictest pattern generation are applied to find the location of the defect in the fabricated chip. The scan generated output files are then fed to the subsequent phases for implementing the DFT (Design for test) flow. In industry there are various other tools are there for the purpose.Finally test coverage is achieved with the help of mentor graphics which is extension of this work.

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