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IMPLEMENTATION OF SINGLE PHASE GRID CONNECTED 15- LEVEL INVERTER WITH MINIMUM NUMBER OF SWITCHES USING PDPWM TECHNIQUE

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Abstract—In this era of modern technology, it has become necessary to supply variable voltages to various loads, whether it is for changing the brightness of a lamp or changing the speed of a motor, which is an inductive load. Use of power electronics for motor drives has become so common that most motors come with the drive circuits. The flip side to using inverter circuits for controlling voltage is that it injects harmonics into the distribution system. So, there is a lot of scope for improvement in the design of inverter circuits. There is constant improvements made in the inverter circuits, so they produce better control of voltage with lesser harmonics being generated. Using switching circuits for Different topologies of converters are leading the way into the medium and high-powered applications of the electric sector, which are undergoing great advancements. Multi-Level Inverters (MLI) are a type of converter that can be used for a wide range of applications by creating appropriate levels of output voltages using a variety of pulse width modulation schemes. With the goal of reducing harmonic content, a fifteen-level inverter is designed in this project work by creating pulse patterns with the aid of Sine wave Pulse width modulation technique and Pulse Disposition (PD) modulation method. MLI is provided with desired switching patterns by developing an appropriate logic gate circuit. This work uses MATLAB/SIMULINK to provide the complete switching pulses through logic circuit which decides the switching pattern. The switching sequence is represented by binary codes. The output voltage waveforms of the inverter circuit, and Total Harmonic Distortion (THD) analysis is presented in this work.

Keywords— Multi-Level Inverter, Pulse Width Modulation, Pulse Disposition Modulation, Total Harmonic Distortion, H-Bridge Inverter

I.   INTRODUCTION

Use of inverters to provide variable voltage has become very common. As a result, keeping harmonics and distortions due to harmonics low has become a challenge. A lot of research has gone into and is still going on to reduce harmonics, if not eliminate it altogether. Earlier inverters were used to mainly to drive lighting loads which are basically resistive. But now a days inverters have to drive loads that are inductive also, which adds to the challenge. Therefore use of Multi-Level Inverters(MUL) are found to be more successful in combating Total Harmonic Distortion(THD) and its effects. Even though they do reduce harmonics, a lot of research has gone into improving the performance of the circuit in terms of NOT ONLY reducing harmonics, but also improve efficiency. This has resulted in various new topologies.

Two and three level inverters are unable to provide higher efficiency and satisfy Grid code requirements for higher power and voltage ratings. Therefore, medium and megawatt scale PV inverters are moving towards multilevel structures. Cascaded H-Bridge type has shown to be more advantageous than other methods and hence PD-PWM modulation technique is implemented on the cascaded H- Bridge multi-level inverter and presented here.

II.   EXISTING SYSTEM

Javad Ebrahimi et al have presented a new topology for cascaded multi-level converter which is based on multiple sublevel converter units and a full bridge converter. This topology reduces the number power electronic devices like power diodes, IGBTs, switches and DC voltage sources. This topology provides a maximum of 400V with 125 levels of voltages. This topology uses 24 IGBTs with a blocking voltage of 604,5 on the bidirectional switches. Using this many number of devices increases the cost and complexity of the circuit while compromising on the reliability of the circuit.

Vasudevan et al have proposed a topology that uses a CUK- KY converter. This CUK converter is integrated with renewable energy sources such as photovoltaic cells or fuel cells. In order to improve the performance of the fuel cell PI control is employed. The CUK-KY converter is integrated with a multi-level inverter in order to reduce harmonics. Z. Bayat et al have proposed a new topology for cascaded

MLI with lesser number of switches and driver circuits which in turn reduces the overall cost of the circuit. The structure presented here has basic inverter units integrated with bidirectional and unidirectional switches. An algorithm is proposed for determining the magnitudes of source DC voltages and another algorithm produces all even and odd levels at the output of the circuit. Advantage of this structure is that, this circuit requires less number of DC voltage sources and the switches have smaller magnitudes of blocking voltages as compared to conventional inverters. This circuit, which is a 21 level inverter circuit, can produce all odd and even voltage levels.

S R Mohapatra et al have presented a scheme which is easy to implement and which can be extended to any higher level inverter without much trouble. Finite Control Set Model Predictive Control is a popular choice for applications that are grid interactive because it is easy to implement and it is simple. But this control is computationally burdensome as it needs all the possible switching states of the inverter. This becomes very complicated and needs addressing while applying this scheme to control multi-level inverters. Therefore, to reduce complexity a S factor scheme for implementing FCSMPC for grid interactive applications is proposed for controlling grid current while balancing the capacitor voltages in neutral point clamped 3-level inverters. This makes it easier to implement. In this scheme predicted reference inverter voltages are derived from predicted grid voltage and current and present value of grid current for suitably chosen redundant switching states at every sampling instant. Then the S factor scheme can be applied to select the switching state that is closest to predicted reference inverter voltage vector at the same sampling instant.

III.   PROPOSED SYSTEM

The topology presented here has 15 levels of operation. By suitably varying the gating signals to the three MOSFET switches at various times the 15 voltage levels are generated. As we can see in Circuit diagram shown in Fig 1, there are three DC sources connected to three MOSFETS and every time the MOSFET gets connected with respective voltage sources, it gets the gate

signal, which turns it on. Then the DC sources provide the respective voltage level to the circuit. In Table 1, the switching pattern is shown with respect to each and every voltage level.
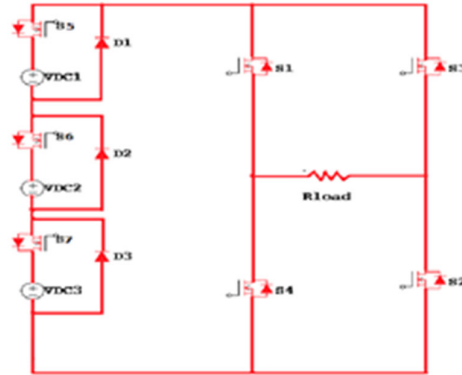

Fig 1. Circuit Diagram of Proposed System

The output voltage of the inverter can be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by Pulse Width Modulation (PWM) control used within the inverter.In this method, a fixed DC input voltage is given to the inverter and a controlled AC output voltage is obtained by adjusting the ON-OFF periods of the inverter components. This is the most popular method of controlling the output voltage and this method is termed as PWM control. In this project, Phase Disposition Pulse Width Modulation has been used. This topology comes under Level Shifted PWM topology. PD-PWM Switching signal for 15 level Inverter is as shown in Fig 2. The switching order of the MOSFET based ON gate signals is as shown in Table 1.
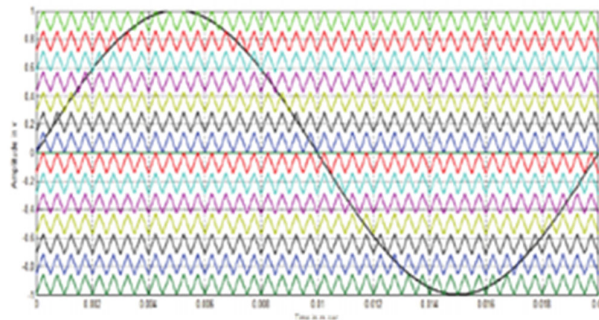

Fig 2. PD-PWM Switching signal for 15 level Inverter

TABLE 1. Switching order of MOSFET based ON gate signals

Vo	S1	S2	S3	S4	S5	S6	S7
V_{DC}	1	1	1	1	1	0	0
$\frac{6V_{DC}}{7}$	0	1	1	1	1	0	0
$\frac{5V_{DC}}{7}$	1	0	1	1	1	0	0
$\frac{4V_{DC}}{7}$	0	0	1	1	1	0	0
$\frac{3V_{DC}}{7}$	1	1	0	1	1	0	0
$\frac{2V_{DC}}{7}$	0	1	0	1	1	0	0
$\frac{V_{DC}}{7}$	1	0	0	1	1	0	0

0	0	0	0	1	0	1	0
0	0	0	0	0	1	0	1
$-\dfrac{V_{DC}}{7}$	1	0	0	0	0	1	1
$-\dfrac{2V_{DC}}{7}$	0	1	0	0	0	1	1
$-\dfrac{3V_{DC}}{7}$	1	1	0	0	0	1	1
$-\dfrac{4V_{DC}}{7}$	0	0	1	0	0	1	1
$-\dfrac{5V_{DC}}{7}$	1	0	1	0	0	1	1
$-\dfrac{6V_{DC}}{7}$	0	1	1	0	0	1	1
$-V_{DC}$	1	1	1	0	0	1	1

IV. SWITCHING MODES FOR 15 LEVEL INVERTER

A. Mode 1- Maximum Positive Output Voltage Vdc

During mode 1, MOSFET Switches S1, S2, S3 & S4 are turned ON, and maximum positive voltage Vdc is applied to the positive terminal (a) of the load. The negative terminal (b) of the load is grounded through the MOSFET Switch S5 which is turned ON, while the remaining switches are in OFF condition.
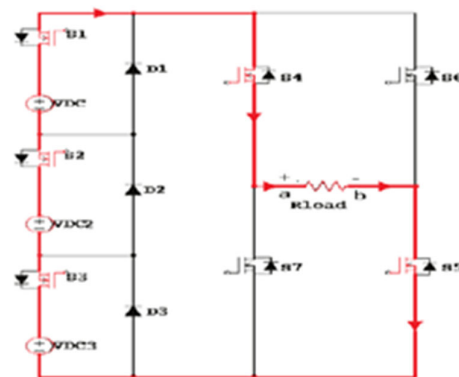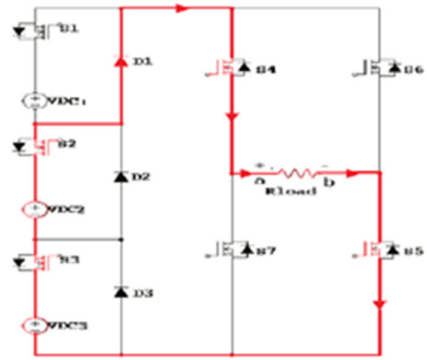

Fig 3. Output Voltage level Vab=Vdc

This is as shown in Fig 3. The current flows through the load from 'a' to 'b', so that the voltage across the load is +Vdc.

B. Mode 2- Positive Output Voltage $+\dfrac{6}{7}V_{dc}$

During mode 2, MOSFET Switches, S2, S3 & S4 are turned ON, while MOSFET Switch S1 is turned OFF and current flows through Diode D1. Therefore, a positive voltage of $+\dfrac{6}{7}V_{dc}$ is applied to the positive terminal (a) of the load. The negative terminal (b) of the load is grounded through the MOSFET Switch S5 which is turned ON, while the remaining switches are in OFF condition.
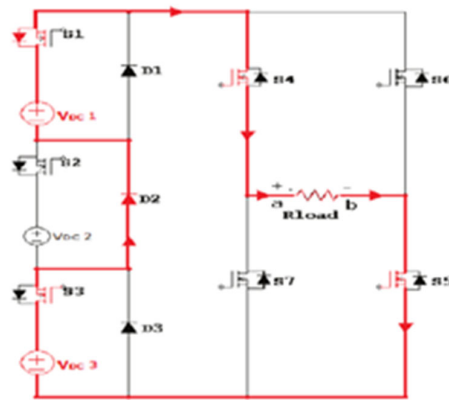
Fig 4. Output Voltage level Vab= $v_{ab}=+\frac{6}{7}V_{dc}$

This is as shown in Fig 4. The current flows through the load from 'a' to 'b', so that the voltage across the load is .

C.   Mode 3- Positive Output Voltage of $+\frac{5}{7}V_{dc}$

During mode 3, MOSFET Switches, S1, S3 & S4 are turned ON, while MOSFET Switch S2 is turned OFF and current flows through Diode D2. Therefore, a positive voltage of $+\frac{5}{7}V_{dc}$ is applied to the positive terminal (a) of the load. The negative terminal (b) of the load is grounded through the MOSFET Switch S5 which is turned ON, while the remaining switches are in OFF condition.

Fig 5. Output Voltage level $v_{ab}=+\frac{5}{7}V_{dc}$

This is as shown in Fig 5. The current flows through the load from 'a' to 'b', so that the voltage across the load is .

D.   Mode 4 - Positive Output Voltage of $+\frac{4}{7}V_{dc}$

During mode 4, MOSFET Switches, S3 & S4 are turned ON, while MOSFET Switches S1 and S2 are turned OFF and current flows through Diodes D1 and D2. Therefore, a positive voltage of is applied to the positive terminal (a) of the load. The negative terminal (b) of the load is grounded through the MOSFET Switch S5 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 6. The current flows through the load from 'a' to 'b', so that the voltage across the load is $+\frac{4}{7}V_{dc}$. .
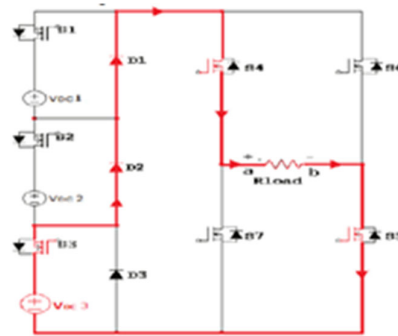
Fig 6. Output Voltage level $V_{ab}=+\frac{4}{7}V_{dc}$

E.   Mode 5- Positive Output Voltage of $+\frac{3}{7}V_{dc}$

During mode 5, MOSFET Switches, S1, S2 & S4 are turned ON, while MOSFET Switch S3 is turned OFF and current flows through Diode D3. Therefore, a positive voltage of $+\frac{3}{7}V_{dc}$ is applied to the positive terminal (a) of the load. The negative terminal (b) of the load is grounded through the MOSFET Switch S5 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 7. The current flows through the load from 'a' to 'b', so that the voltage across the load is $+\frac{3}{7}V_{dc}$..
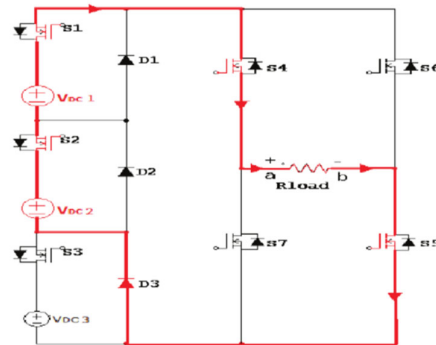

Fig 7. Output Voltage level Vab=

F.   Mode 6- Positive Output Voltage of $+\frac{2}{7}V_{dc}$

During mode 6, MOSFET Switches, S2 & S4 are turned ON, while MOSFET Switches, S1 and S3 are turned OFF and current flows through Diodes D1 and D3. Therefore, a positive voltage of $+\frac{2}{7}V_{dc}$ is applied to the positive terminal (a) of the load. The negative terminal (b) of the load is grounded through the MOSFET Switch S5 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 8. The current flows through the load from 'a' to 'b', so that the voltage across the load is $+\frac{2}{7}V_{dc}$..
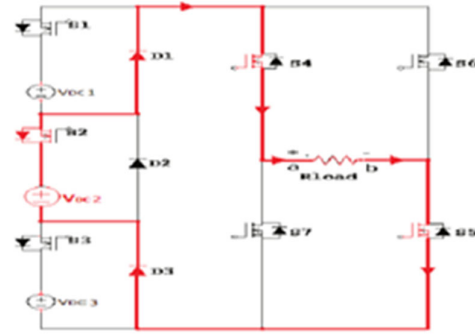
Fig 8. Output Voltage level $V_{ab}=+\frac{3}{7}V_{dc}$

G.   Mode 7- Positive Output Voltage of $+\frac{1}{7}V_{dc}$

During mode 7, MOSFET Switches, S1& S4 are turned ON, while MOSFET Switches S2 and S3 are turned OFF and current flows through Diodes D2 and D3. Therefore, a positive voltage of $+\frac{1}{7}V_{dc}$ is applied to the positive terminal (a) of the load. The negative terminal (b) of the load is grounded through the MOSFET Switch S5 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 9. The current flows through the load from 'a' to 'b', so that the voltage across the load is $+\frac{1}{7}V_{dc}$..
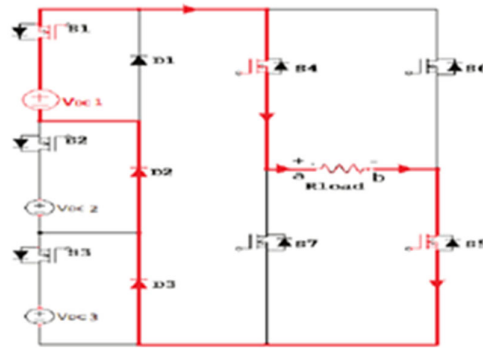

Fig 9. Output Voltage level $V_{ab}=+\frac{1}{7}V_{dc}$

H.   Mode 8- Positive Output Voltage of $-\frac{1}{7}V_{dc}$

During mode 8, MOSFET Switches, S7 & S5 or switches S6 and S4 are turned ON. Therefore, 0V is applied to the positive terminal (a) of the load and no current flows through the load. The circuit is as shown in Fig 10.
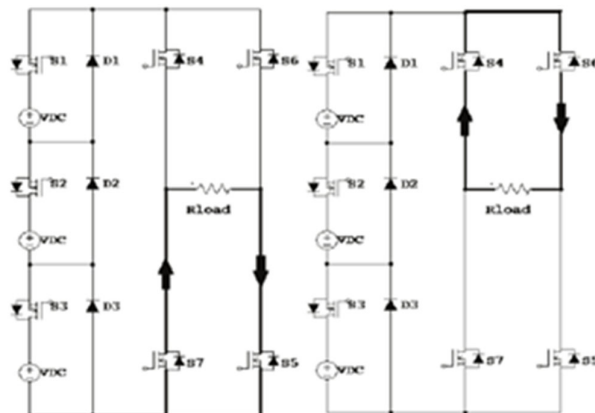
Fig 10. Output Voltage level Vab=

I. Mode 9- Negative Output Voltage of $-\frac{1}{7}V_{dc}$

During mode 9, MOSFET Switches, S1and S6 are turned ON, while MOSFET Switches S2 and S3 are turned OFF and current flows through Diodes D2 and D3. Therefore, a positive voltage of   is applied to the negative terminal (b) of the load. The positive terminal (a) of the load is grounded through the MOSFET Switch S7 which is turned ON, while the remaining switches are in OFF condition. This is as shown in   Fig 11. The current flows through the load from 'a' to 'b', so that the voltage across the load is .

Fig 11. Output Voltage level Vab=

J. Mode 10- Positive Output Voltage of $-\frac{2}{7}V_{dc}$

During mode 10, MOSFET Switches, S2 and S6 are turned ON, while MOSFET Switches S1 and S3 are turned OFF and current flows through Diodes D1 and D3. Therefore, a positive voltage of $+\frac{1}{7}V_{dc}$ is applied to the negative terminal (b) of the load. The positive terminal (a) of the load is grounded through the MOSFET Switch S7 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 12. The current flows through the load from 'a' to 'b', so that the voltage across the load is $-\frac{1}{7}V_{dc}$. .
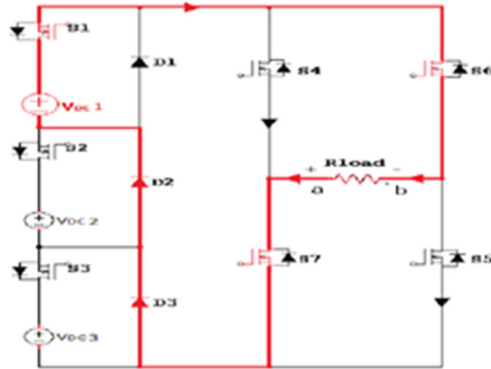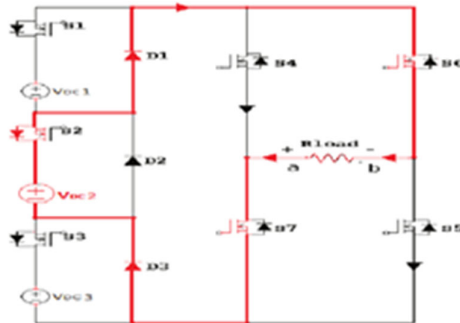

Fig 12. Output Voltage level $V_{ab}=-\frac{2}{7}V_{dc}$

K. Mode 11- Positive Output Voltage of $-\frac{3}{7}V_{dc}$

During mode 11, MOSFET Switches, S1, S2 and S6 are turned ON, while MOSFET Switch S3 is turned OFF and current flows through Diode D3. Therefore, a positive voltage of   is applied to the negative terminal (b) of the load. The positive terminal (a) of the load is grounded through the MOSFET Switch S7 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 13. The current flows through the load from 'a' to 'b', so
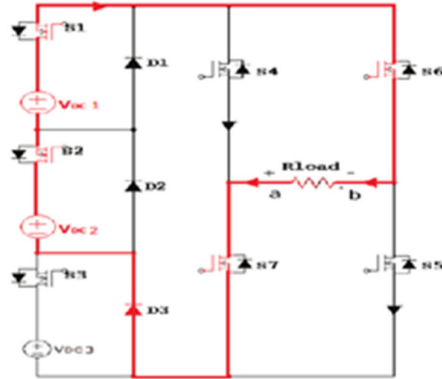
that the voltage across the load is .

Fig 13. Output Voltage level $V_{ab} = -\frac{3}{7}V_{dc}$

L.   Mode 12- Positive Output Voltage of $-\frac{4}{7}V_{dc}$

During mode 12, MOSFET Switches, S3 and S6 are turned ON, while MOSFET Switches S1 and S2 are turned OFF and current flows through Diodes D1 and D2. Therefore, a positive voltage of $+\frac{4}{7}V_{dc}$ is applied to the negative terminal (b) of the load. The positive terminal (a) of the load is grounded through the MOSFET Switch S7 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 14. The current flows through the load from 'a' to 'b', so that the voltage across the load is $-\frac{4}{7}V_{dc}$.

Fig 14. Output Voltage level Vab=

M.   Mode 13- Positive Output Voltage of $-\frac{5}{7}V_{dc}$

During mode 13, MOSFET Switches, S1, S3 and S6 are turned ON, while MOSFET Switch S2 is turned OFF and current flows through Diode D2. Therefore, a positive voltage of $+\frac{5}{7}V_{dc}$ is applied to the negative terminal (b) of the load. The positive terminal (a) of the load is grounded through the MOSFET Switch S7 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 15. The current flows through the load from 'a' to 'b', so that the voltage across the load is $-\frac{5}{7}V_{dc}$.
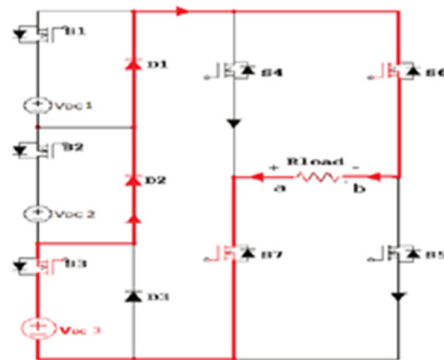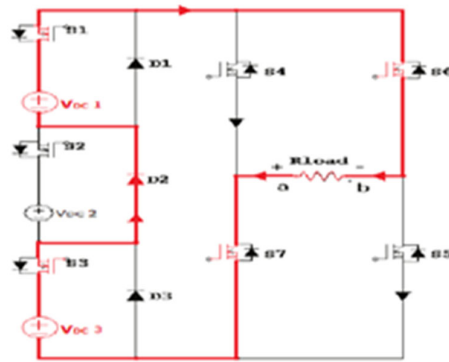
Fig 15. Output Voltage level $v_{ab} = -\frac{5}{7}V_{dc}$

N.   Mode 14- Positive Output Voltage of $-\frac{6}{7}V_{dc}$

During mode 14, MOSFET Switches, S2, S3 and S6 are turned ON, while MOSFET Switch S1 is turned OFF and current flows through Diodes D1. Therefore, a positive voltage of $+\frac{6}{7}V_{dc}$ is applied to the negative terminal (b) of the load. The positive terminal (a) of the load is grounded through the MOSFET Switch S7 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 16. The current flows through the load from 'a' to 'b', so that the voltage across the load is $-\frac{6}{7}V_{dc}$
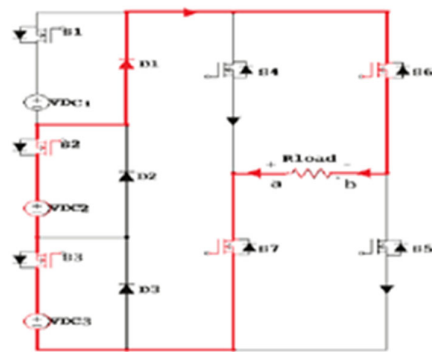

Fig 16. Output Voltage level Vab=

O.   Mode 15- Positive Output Voltage of

During mode 15, MOSFET Switches S1, S2, S3 & S6 are turned ON, and so maximum positive voltage Vdc is applied to the negative terminal (b) of the load. The positive terminal (a) of the load is grounded through the MOSFET Switch S7 which is turned ON, while the remaining switches are in OFF condition. This is as shown in Fig 17.

Fig 17 - Output Voltage level Vab=

V.   RESULTS OF SIMULATION AND CONCLUSION

This system is designed to provide an output close to an ac waveform with minimum total harmonic distortion. The circuit was simulated using MATLAB Simulink software. The circuit that was simulated is as shown in Fig 18.

Fig 18 – Circuit Diagram Simulated on MATLAB SIMULINK

The order in which the switches are turned ON or OFF depends on the gating pulses given to

the MOSFET switches. The output of the gating pulses which are PWM PI pulses, which are simulated for the 15 Voltage levels are as shown in Fig 19.

Fig 19. Simulated PWM-PI modulated gating pulses
The simulated output waveform of the 15 level inverter, is as shown in the Fig 20.

Fig 20. Output Waveform of simulated 15 level Inverter
The simulated result shows a wave form that resembles a sinusoidal waveform, which a normal ac voltage resembles. The load simulated is a motor and the motor torque and speed obtained during simulation is shown in Fig 21. The simulated motor current obtained is shown in Fig 22.

Fig 21 Motor Speed and Torque with motor input from 15 level Inverter

Fig 22 Motor current with motor input from 15 level Inverter
The total harmonic distortion (THD) of this waveform is analysed using FFT analysis. Ideally THD should be as low as possible. The percentage (%) of THD in a voltage or current waveform determines the quality of the voltage or current. The results of THD analysis of voltage and current waveforms are presented in Fig 23 and Fig 24.

Fig 23 Harmonic Content in the Inverter Output Voltage

Fig 24 Harmonic Content in the Inverter Output Current
The simulated results show a total harmonic distortion of 7.92% for the voltage waveform and a total harmonic distortion of 3.67% for the current waveform, which is quite low. Increasing the number of voltage levels can reduce the total harmonic distortion, but that will increase the circuit complexity by having to increase the number of power electronic switches like MOSFETs or IGBTs used in the circuit.

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