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PERFORMANCE EVALUATION OF PV INTEGRATED GRID SYSTEM USING SEVEN-LEVEL GRID-CONNECTED PACKED U CELL INVERTER

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Abstract
This article presents and analyses the standalone operation of a Packed U Cell(PUC) inverter in a grid-connected PV system. In this system, seven level inverter ifs formulated using six switches and two DC sources. The INC MPPT topology is utilized in this topology to boost the efficiency of the PV system and is integrated with a SEPIC converter. To demonstrate its effectiveness, simulations were carried out using the MATLAB/Simulink platform. From the results, it can be concluded that the proposed PUC7 inverter injects an active with unit power factor at the grid.

Introduction
The use of fossil fuels as a source for electrical energy production has resulted in increased fuel costs and carbon dioxide emissions. On the other hand, Renewable Energy Sources (RES) like PV, wind etc., plays a significant role in electricity generation. Solar PV cell power generation is characterised by low operating costs, clean energy and less maintenance. Apart from this, PV based energy systems are a possible solution to the growing environmental concerns [1]. Due to its ease of installation and operation, PV arrays are used widely in off-grid applications [2]. So researchers from all over the world are currently concentrating on improving the three following aspects of a solar system:
(1) System Efficiency;
(2) Installation Costs and
(3) Reliability.
For integrating PV system with grid, Multilevel inverters are utilised to provide high power form a medium voltage source. They are becoming more popular due to their benefits over traditional inverters. Different voltage levels are synthesised to produce multilevel output [3]. Despite not having a pure sinusoidal output voltage, they have a significantly lower total harmonic distortion (THD) than the two-level topology, which mitigates power quality problems [4].The multilevel inverter can reduce the level of Harmonics at the point of common coupling in accordance with IEEE standard (519-2014). The harmonics limit is fixed at 5% for

current waveforms and 8% for voltage waveforms [5] by this standard. However, when compared to conventional multilevel inverters, packed U-cell (PUC) inverters offer a variety of benefits, including a low device count [6], simplified control and generally good power quality [7–11]. The PUC multilevel inverters were launched in 2008 [12–15].Compared to multilevel inverters, the PUC seven-level inverter has a simplified construction and requires a single capacitor and DC source for the same output voltage levels in the ML[15–20].
Hence, this article proposes a Seven Level PUC inverter for PV systems connected with grid. Figure 1 displays the comprehensive model of the system developed in the current study.

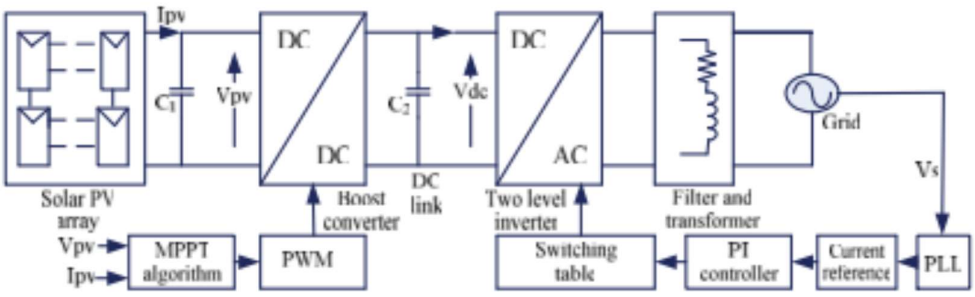


Figure 1. Complete model of the proposed system

It consists of PV modules, the SEPIC converter and PUC converter with the MPPT tracking algorithm.

Methodology

Packed U cell- Design analysis

The architecture of proposed PUC shown in Figure 2, comprises a two complementary switches and a capacitor.
Thus, 2n combinations can be obtained for n cells using n switches and (n-1) capacitors. As a result, the number of levels is equal to 2n-1. Therefore, 6 switches with 2 capacitors are utilized to achieve seven levels.

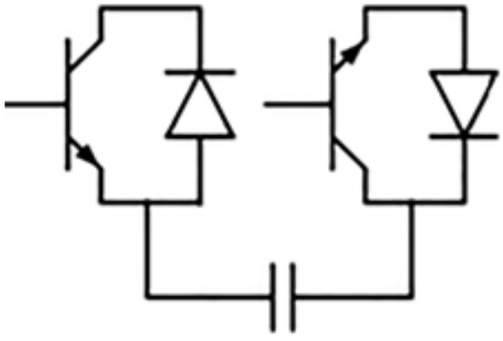


Figure 2. PUC converter (Single Unit)

The voltage obtained using 6 switches, a fixed voltage source and a capacitor must be equal to 1/3 bus voltage (Uc=Udc/3). One leg of the proposed PUC inverter is shown in Figure 3.

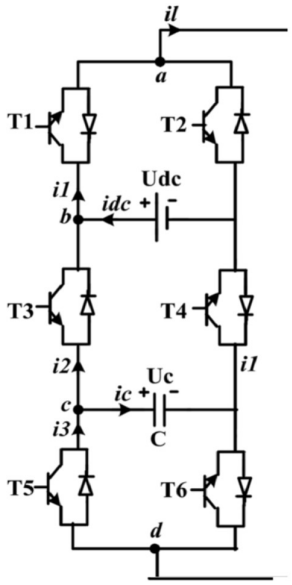


Figure 3. Packed cell inverter for one phase

Thus, the operating stages of single phase inverter are depicted in figure 4.

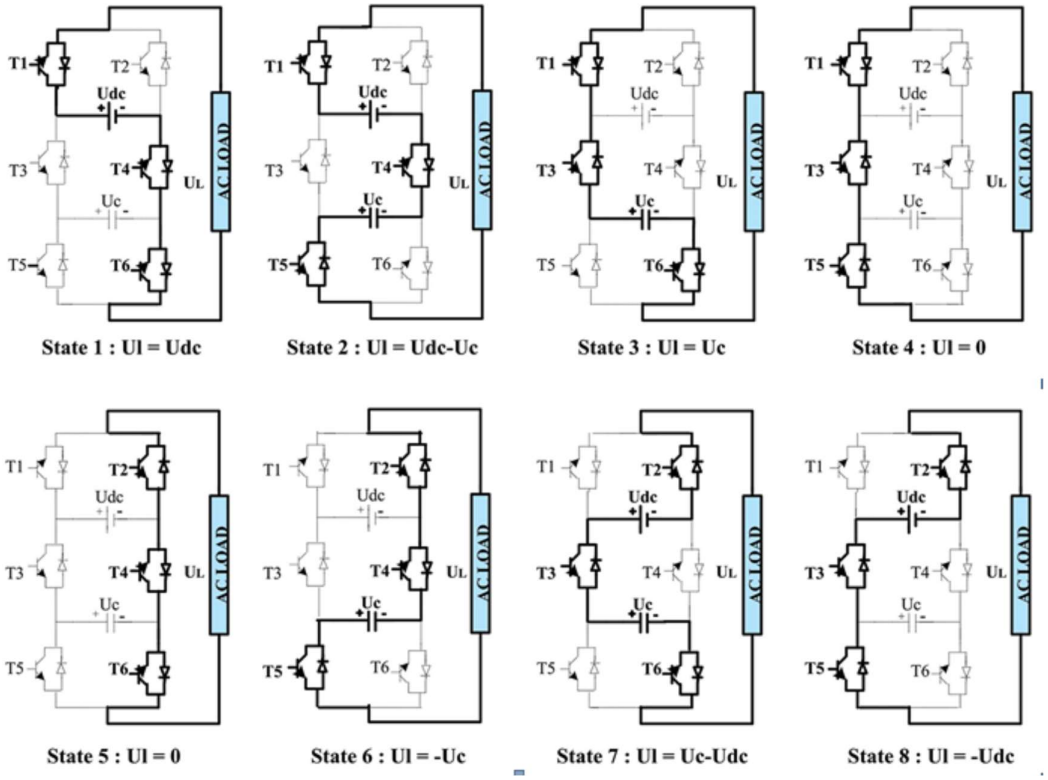


Figure 4. Operating states of one leg

Thus, the output voltage obtained from the above stages are depicted in table 1

Table 1.Voltage levels

States	$T1$	$T3$	$T5$	Uad
1	1	0	0	Udc
2	1	0	1	$Udc - Uc$
3	1	1	0	Uc

4	1	1	1	0
5	0	0	0	0
6	0	0	1	$-Uc$
7	0	1	0	$Uc - Udc$
8	0	1	1	$-Udc$

Design of PV

In this topology, a solar PV array with a output of 2 kW under STC (1000 W/m^2, 25°C) has been utilized. Table 2 illustrates the specifications of this module.

Table 2.Specifications of PV panel

Parameters	**Values**
Maximum Power	250Watts
Voc	37.3
Vmp	30.7
Isc	8.66
Imp	8.15

Design of Converter (SEPIC Converter)

Fig. 5 depicts the DC/DC converter. Inductors (L_1 and L_2), a diode, Capacitors(C_1 and C_2) and a switch (S) constitutes the proposed SEPIC converter.

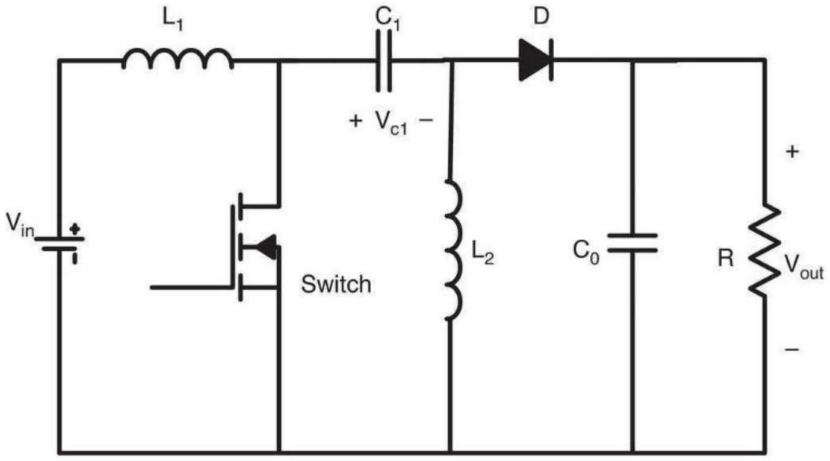
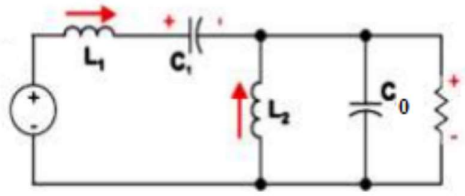
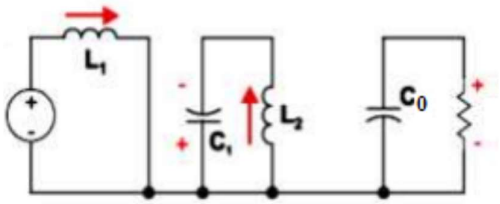


Figure.5. Circuit diagram of the SEPIC converter

Analysis of operating modes of the proposed converter



(a) Switch ON condition



(b) Switch OFF condition

Figure 6. Equivalent circuit diagram (Under switch is ON and OFF condition)

Figure 6 (a and b) depicts the operation of the circuit during on and off cycles of the power switch (respectively in Figures). When the switch is activated, the source charges the input inductor and the first capacitor charges the second inductor. The load capacitor is not receiving any power at this time. The polarities of the inductor current and capacitor voltage are indicated in this figure.

The energy stored in the inductor is transferred to when the power switch is switched off. As seen in Figure 4b, the energy that is stored in inductor is transmitted to the diode and then supplies the energy to the load. During this period, the second inductor is connected to the load. The duty cycle and parasitic components in the circuit play a major role SEPIC's output voltage.

Thus, the voltage gain of the circuit

$$V_0 = \frac{D}{1-D} V_{in} \qquad (1)$$

Selection of Inductor

The inductor ripple current (I_L) must be taken into account while designing an inductor. Consequently, it can be determined using a formula.

$$\Delta(I_L) = 30\% \times \left(\frac{I_{in}}{\eta}\right) \qquad (2)$$

$$L_1 = L_2 = 1/2 \times \left(\frac{V_{in} \times (D)}{\Delta(I_L) \times (fs)}\right) \qquad (3)$$

Selection of Capacitor

Similarly, the output capacitor can be calculated using the formula

$$C_1 = \frac{I_{out} \times (D_{max})}{\Delta(V_{cp} \times (f_s)} \qquad (4)$$

Thus, the design limits of the components incorporated during simulation is tabulated in table 2.

Table 3. Design parameters of the proposed converters and their values

Parameter	Values
L1,L2	0.0017H
C1	4.5952e-6
C2	500e-6
Vin	200
Vout	600
fs	100e3

Design of INC Algorithm

According to MPP and as shown in Fig. 7, an INC topology terminal voltage of the array is controlled by the PV module's incremental and instantaneous conductance values. Equation provides the incremental conductance approach (5).

$$\frac{dI}{dV} = -\frac{1}{V} \text{At MPP}; \qquad \frac{dI}{dV} > -\frac{1}{V} \text{ Left of MPP}; \qquad \frac{dI}{dV} < -\frac{1}{V} \text{Right of MPP} \tag{5}$$

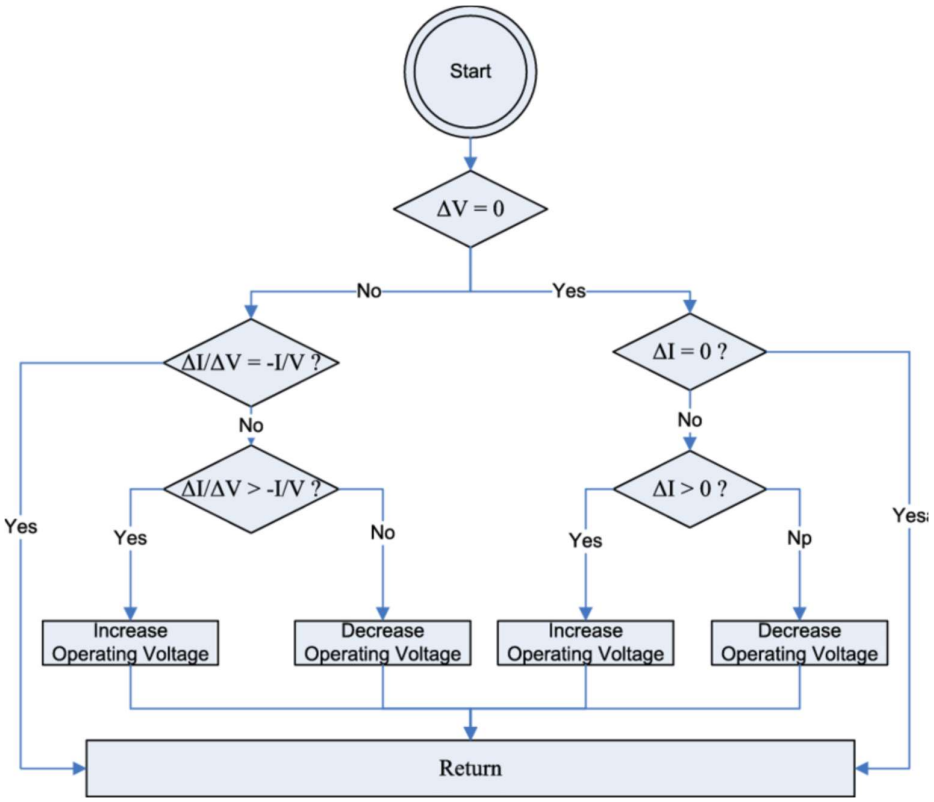


Figure. 7. Flowchart of INC method

Control system

The active and reactive power exchange with the network is managed by the control systems. In order to obtain the phase-shift angles, the grid voltages are supplied to the PLL. The measured angle will be multiplied with the desired phase shift for each phase to keep the power factor within acceptable limits.

To regulate the amount of power injected into the network, maximum reference current (I_m) is multiplied with the unit sinusoidal wave. To reduce the steady-state error, the reference current (I) is compared with the measured current (Is) and delivered to a PI controller. In order to obtain the necessary signal, the reference voltage is compared with carrier voltage and the output voltage of the inverter is obtained.

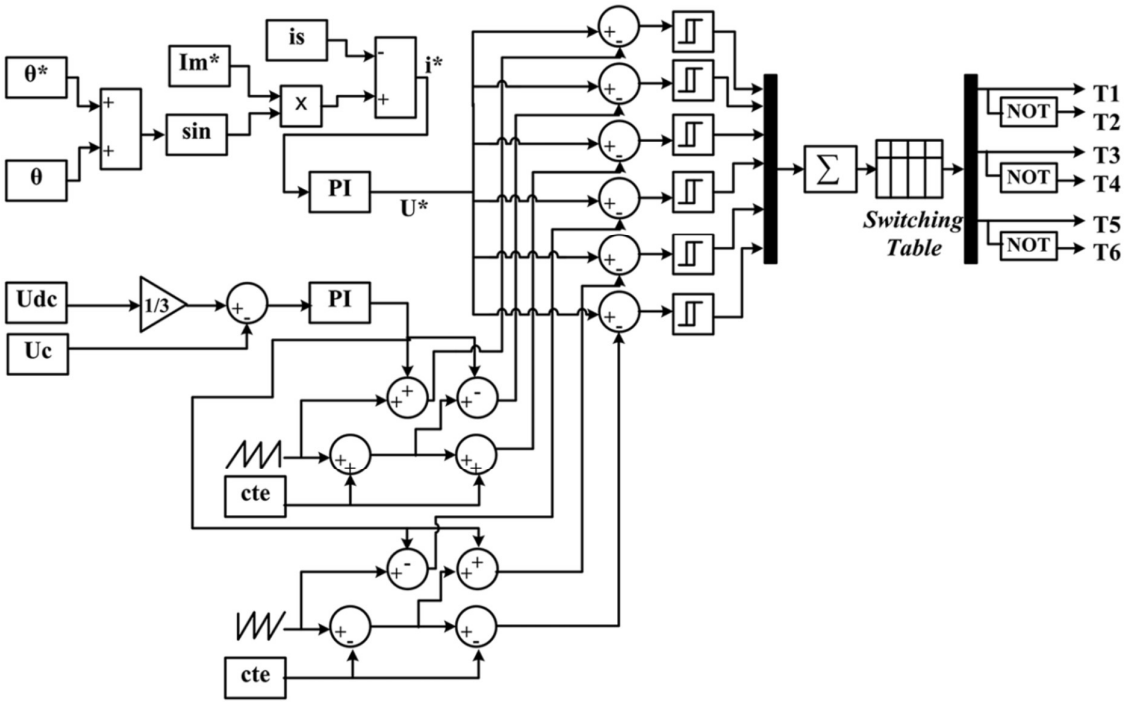


Figure 8. Controller for PWM generation

Results and Discussion

Here, the performance of the simulated system is verified using Matlab/Simulink. The output obtained from the proposed PV array is shown in figure 9.

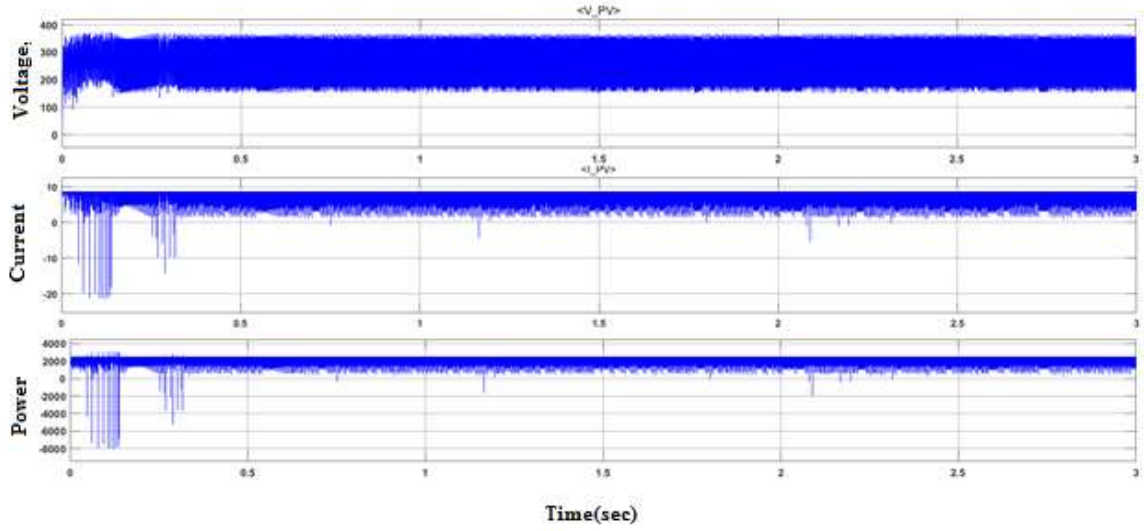


Figure 9. Output obtained from PV

The INC MPPT architecture can track maximum power under constant irradiation, as can be seen from the graph above. The suggested SEPIC converter raises this tracked voltage to 500 V. Figure 10 showed the step-up converters' output voltage waveforms, duty cycle and power output of the converter.

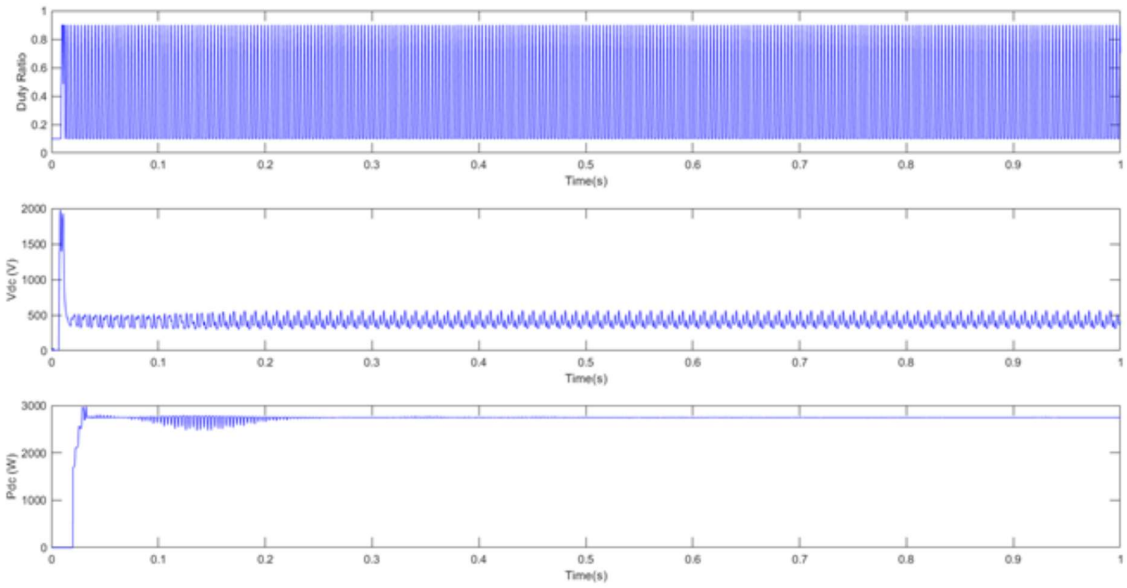


Figure 10.Output of the DC converter

The output from SEPIC is integrated to grid through PUC-7 inverter. An auxiliary capacitor is used to obtain a second voltage source. The inverter's output voltage waveform is depicted in Fig. 11.

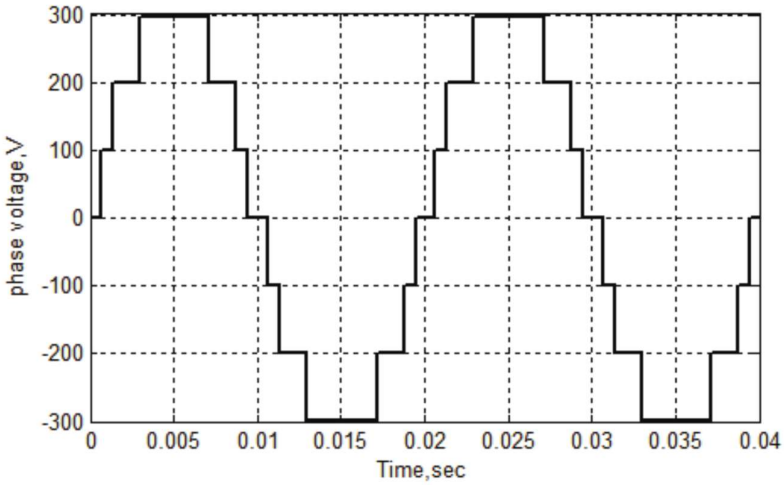


Figure 11.Output of the packed cell inverter.

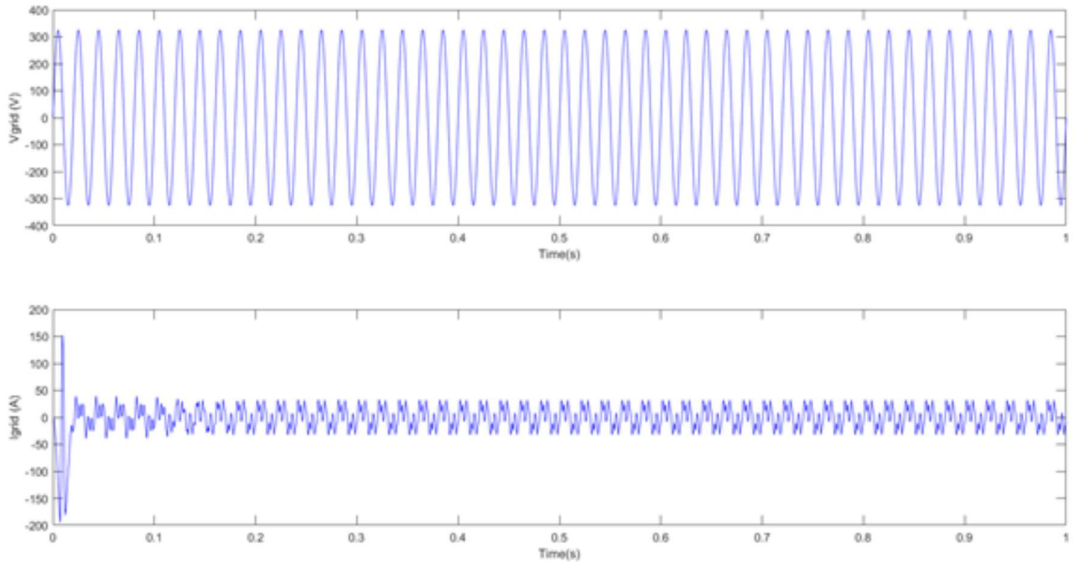


Figure 12. Grid side waveforms (voltage and current)

The current and voltage f the grid is shown in Fig. 12. As a result of producing higher voltage levels, PUC 7 inverter is anticipated to produce a lower harmonics at the grid side when compared to conventional inverters.

Conclusion

The suggested PUC inverter has the ability to produce an output voltage waveform with seven levels and low harmonic content. The introduced topology has been created with a lower switching frequency aspect, and the corresponding switching algorithm has been implemented. Other benefits of PUC deployment include decreased production costs and smaller packages as a result of smaller filters.

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