Semiconductor Optoelectronics, *Vol. 41 No. 12 (2022), 1678-1685*
https://bdtgd.cn/

PERFORMANCE ANALYSIS OF A 1-BIT FULL ADDER CIRCUIT USING 18 TRANSISTORS AND CNFET TECHNOLOGY

Dr. A S Rathore
Research Guide, Dept. of Electronics and Communication Engineering, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Bhopal-Indore Road, Madhya Pradesh, India

Latha Yallanki
Research Scholar, Dept. of Electronics and Communication Engineering, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Bhopal-Indore Road, Madhya Pradesh, India

Abstract
This research proposes a novel approach to designing a 1-bit full adder circuit using 18 transistors, integrating Carbon Nanotube Field-Effect Transistor (CNFET) technology, complementary metal oxide semiconductor (CMOS), pass transistor logic (PTL), and transmission gate logic (TGL). The critical route delay, a key metric for assessing circuit speed and efficiency, is optimized by strategically combining these logic types. The experimental setup, simulated using 32 nm CNFET technology in the Cadence Virtuoso CAD tool, demonstrates superior performance compared to traditional circuits in terms of power, delay, and power-delay product. The proposed circuit outperforms the farthest and nearest candidates by 68.5%, 70%, and 68.3%, and 19.4%, 2.06%, and 22.3%, respectively. Analysis of transistor count, leakage current, static power, dynamic power, and total power consumption further validates the efficiency of the proposed 18T-FA circuit.

Introduction
The continuous evolution of portable electronic gadgets is closely tied to the increased integration of diverse multimedia hardware. As these devices become more sophisticated, their demand for power grows, necessitating the development of energy-efficient and area-efficient digital integrated systems. Among the critical components in these systems are full adders (FAs), particularly in advanced communication systems like Digital Signal Processors (DSPs). In state-of-the-art communication systems, FAs play a crucial role in various applications, such as the final carry propagate paths in multiplication and division circuits. Additionally, FAs find specific use in building blocks of communication systems, such as "direct-digital-frequency synthesizers" (DDFS). Figure 1 illustrates the power distribution among different functional blocks in a high-frequency DDFS circuit commonly required in Long-Term-Evolutionary (LTE) communication systems.

In the context of this figure, the "phase accumulator and complementary" block, which involves arithmetic circuits, stands out as a power-hungry element, demanding special attention. This observation underscores the need for optimization of a 1-bit FA for context-based applications,

making it an ongoing and essential process. Specifically, the focus is on enhancing the efficiency of FAs for applications like DDFS in LTE communication systems, where power consumption is a critical concern.

The classification of Full Adder (FA) architectures into two main types: "carry-independent-sum-adders" (CISAs) and "carry-dependent-sum-adders" (CDSAs). The focus then shifts to the further classification of FAs into static, dynamic, and hybrid FAs based on the type of logic style employed.

Static CMOS and its variant, the static CMOS mirror adder, are highlighted as examples of CDSAs. These adders are recognized for their full swing outputs and reliability even at low supply voltages. However, they suffer from drawbacks, notably speed degradation due to the substantial gate capacitance at each input. Each input has to drive a gate capacitance of both a pMOS and an nMOS device. The presence of pMOS pull-up circuitry further contributes to speed issues because pMOS devices are slower than nMOS devices. To compensate for this speed difference, pMOS devices need to be sized up, leading to increased area and higher power dissipation. Additionally, the static CMOS FAs consume more transistors, resulting in a larger area due to increased total capacitance (TC).

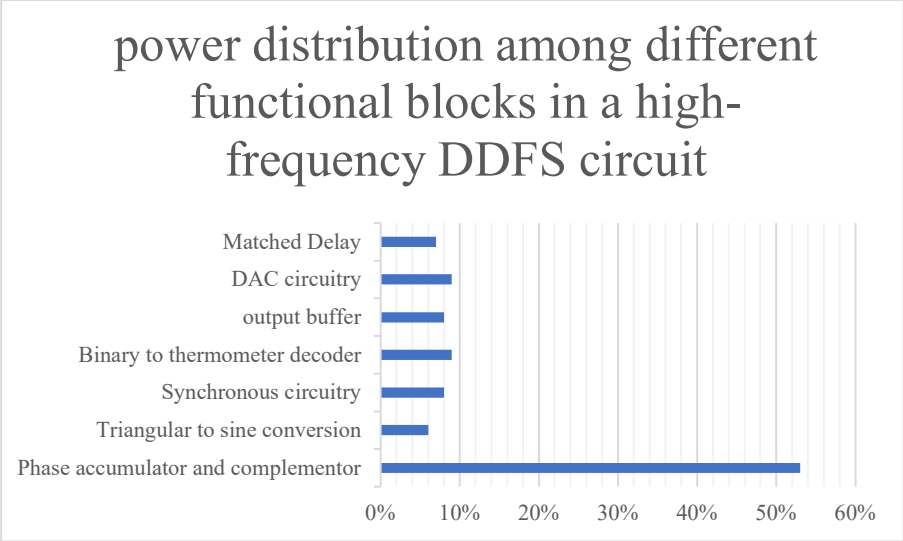

Figure 1. Power distribution among different functional blocks in a high-frequency DDFS circuit

The "transmission-gate-adder" (TGA), 14T, 8T, and "transmission-function-adder" (TFA) are all low-power adders due to their low total capacitance (TC). The 14T adder is based on Pass-Transistor Logic (PTL) and Transmission Gate (TG) logics, while the 8T adder is derived solely from PTL logic. Both TFA and TGA are based on TG logic. However, a drawback of these adders is their lack of driving capability, which is crucial in long chain adders.

Another category of adders discussed is the "hybrid-pass-transistor-with-static-CMOS logic" (HPSC-1) and its improved version, HPSC-2. These adders aim to balance different logic styles to trade-off between different dynamic metrics (DMs) and achieve low TC. However, they suffer from layout complexity due to the different sizing of pMOS and nMOS devices. The Hybrid-1 FA, a subtype of HPSC-1, offers good driving capability and better noise margin due

to the combination of pass transistor and static CMOS design. Nevertheless, it exhibits relatively higher power dissipation attributed to glitches associated with internal node capacitances and increased silicon area due to different sizes of pMOS and nMOS transistors. Two other types of adders mentioned are the "double-pass-logic" (DPL) and "swing-restoring-complementary-pass-transistor-logic" (SRCPL), which combine low power and high speed. However, they suffer from large silicon area requirements due to higher TC. The Hybrid-2 adder, also known as the 1-bit FA, is reported to have low power, high speed, and low TC. It is based on the Complementary Inverter Structure (CIS), achieving the desired performance through transistor sizing, albeit at the cost of extra area.

Proposed Methodology

A digital logic circuit called a complete adder performs mathematical addition. Adders are a fundamental component of on-chip libraries and are used to compute operations like table indices, addresses, and other related tasks. The two input operands (A, B) and previous stage carry are added to produce the resultant sum and carry output of a complete adder (Cin). Figure 2 displays a block diagram of a 1-bit complete adder.

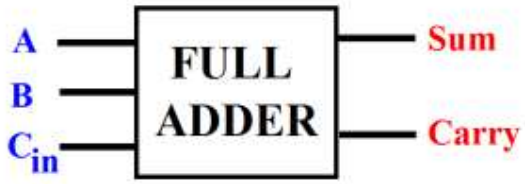

Figure 2: Block diagram of 1-bit Full Adder

The relationship between input and output bits can be expressed with expressions given in equation (1) and (2). The truth table of a 1-bit full adder is shown in Table 1.

$$SUM = ABC_{in} + \overline{AB}C_{in} + \overline{A}B\overline{C}_{in} + A\overline{BC}_{in}$$

$$CARRY = AB + BC_{in} + AC_{in}$$

Where A and B are the inputs and the outputs are SUM and CARRY while Cin represents the carry input if any.

Table 1: Truth Table of Full Adder

A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

There are various methods to build a circuit that is efficient with power, but the optimal one is to minimize the number of transistors and the latency on the critical information line leading

to the output. Each of the resulting circuits has its own set of benefits and drawbacks. We have considered power, delay, and power-delay product as the parameters to compare in order to get a firm conclusion on the relative merits of different systems. The aforementioned parameter was selected on the basis that it would provide the greatest breadth of coverage across all of the necessary qualities, including but not limited to type problem, power consumption, responsiveness, suitability for purpose, etc. Multiple implementations of the designed circuits are carried out using Pass semiconductor unit Logic (PTL) and Transmission Gate Logic (TGL). Pass-transistor logic's simplified design, signal re-use, and negligible impact on static power are all pluses, while transmission logic's adaptability in reducing both transistor count and parasitic effects is a major selling point.

Full Adder with 18 Transistor (18T-FA)

The utilization of CNFET (Carbon Nanotube Field-Effect Transistor) technology in realizing a specific circuit employing 18 transistors, as depicted in Figure 2. This circuit represents a 1-bit full-adder and is ingeniously crafted by integrating complementary metal oxide semiconductor (CMOS), pass transistor logic (PTL), and transmission gate logic (TGL).

The core of the proposed 18T full-adder circuit involves the incorporation of CMOS logic in the intermediate stages, utilizing C1-C10 transistors. Furthermore, the circuit employs PTL logic, comprised of C11-C14 transistors, to generate the SUM output, while the CARRY output is produced through TGL logic, involving C15-C18 transistors.

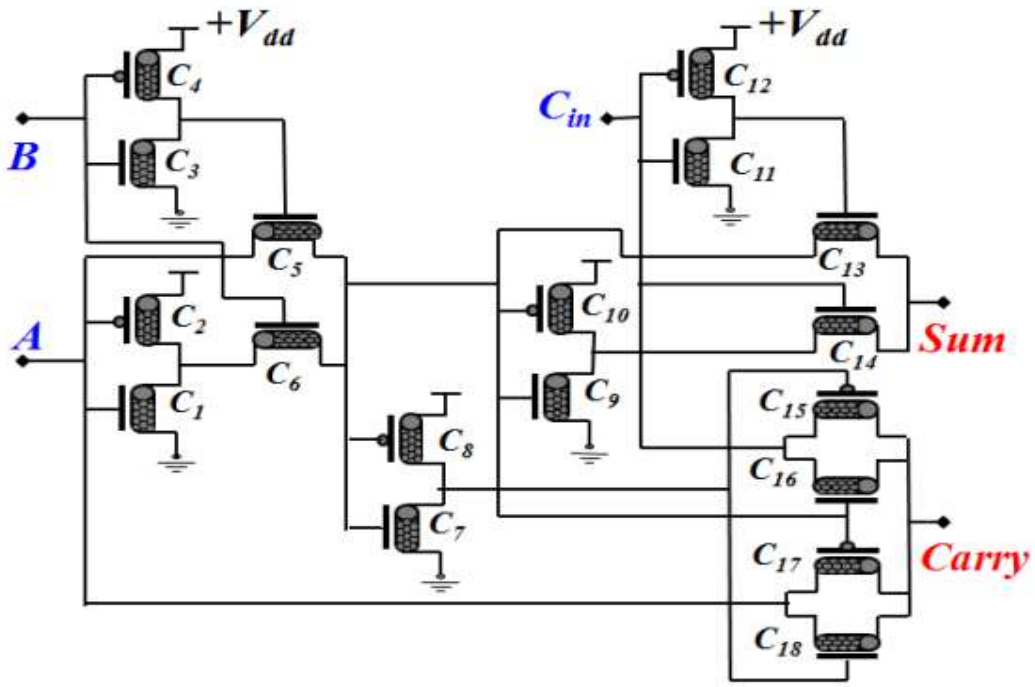

Figure 3: Schematic diagram of 18T-FA

Proposed feature of this circuit is its critical route delay, which is determined by the delay introduced by 4 transistors. This critical route delay metric is crucial in assessing the speed and efficiency of the circuit, with lower values generally indicating better performance.

In essence, the integration of CNFET technology along with a strategic combination of CMOS, PTL, and TGL logics allows for the creation of a compact 1-bit full-adder circuit with a total

of 18 transistors. This demonstrates a sophisticated approach to circuit design, optimizing the strengths of each logic type for specific stages within the circuit to achieve the desired functionality and performance.

Result and Discussion

32 nm CNFET technology was used in the experimental setup for the simulation of the suggested designs using the Cadence Virtuoso CAD tool, with the supply voltage being +0.9V, the threshold voltage being 0.289V, and the chirality vector (19, 0). Simulation waveform of the proposed (18T-FA) full adder circuits consists of inputs (A, B, Cin) and outputs (Sum and Carry) are shown in Figure 4.

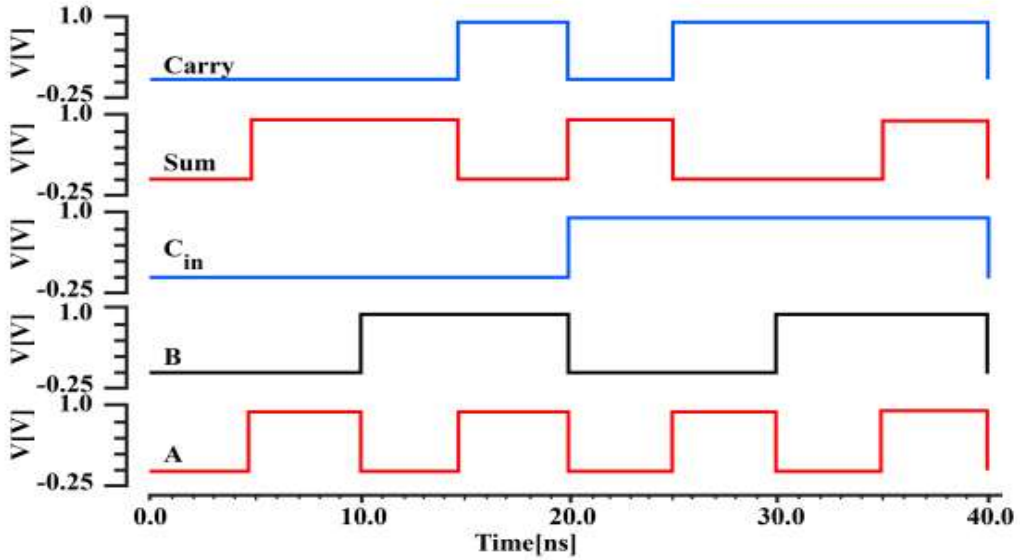

Figure 4: Waveform of 18T-FA

The projected 18T-FA circuit is compared with the traditional circuits and located to be 68.5 %, 70 %, and 68.3 the best than the farthest candidate and 19.4 %, 2.06 %, 22.3 the best than the nearest candidate in terms of power, delay and power-delay product, severally. These full adders circuit styles are compared in terms of semiconductor count, power, delay, and power-delay product. The subsequent points are inferred from the Table 2.

Table 2: Comparison between proposed and other full adders in terms of transistor count, delay, power and power delay product (PDP).

Full Adder Designs	Transistor Count	Power (μ W)	Delay (ps)	PDP (aJ)
C-CMOS [82], 1988	28	0.124	12.355	1.532
TGA [82], 1988	20	0.135	10.104	1.364
TFA [83], 1992	16	0.109	11.701	1.275
CPL-TG [84], 1996	36	0.139	14.26	1.982
Mirror [85], 1997	28	0.126	12.321	1.552
SERF [86], 1999	10	3.326	9852.7	32770.08
13A [87], 2002	10	5.819	9507.8	55325.88
HPSC [88], 2005	26	0.095	30.654	2.912
NEW-HPSC [89], 2006	24	0.123	30.232	3.718
CLRCL [90], 2007	10	5.903	231.18	1364.65
Ours1 [91], 2011	28	0.163	10.866	1.771
HCTG [92], 2015	16	0.124	12.116	1.502
RSD-FA [93], 2016	26	0.091	9.427	0.857
18T-FA [94], 2017	**18**	**0.088**	**8.93**	**0.785**
HMTFA [95], 2018	23	0.121	16.909	2.056
16T-FA	**16**	**0.073**	**8.122**	**0.592**
14T-FA	**14**	**0.052**	**6.469**	**0.336**
12T-FA	**12**	**0.039**	**6.876**	**0.268**

Further analysis of leakage current, static power, dynamic power, and total power consumption is done for the proposed (18T-FA, 16T- FA, 14T-FA and 12TFA) 1-bit full adder designs shown in table 3.

Table 3: Analysis of leakage current, static power, dynamic power and total power consumption.

Proposed Designs	Leakage Current (nA)	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)
18T-FA	0.511	0.462	88.390	88.852
16T-FA	0.349	0.316	73.390	73.706
14T-FA	0.238	0.225	52.750	52.975
12T-FA	0.218	0.197	39.391	39.588

Conclusion

The integration of CNFET technology and a strategic combination of CMOS, PTL, and TGL logics in the proposed 18T full-adder circuit showcases a sophisticated and efficient design approach. The critical route delay, determined by only 4 transistors, emphasizes the circuit's speed and performance. Simulation results using 32 nm CNFET technology reveal that the proposed circuit outperforms traditional counterparts, demonstrating significant advantages in terms of power, delay, and power-delay product. The comprehensive analysis, including transistor count and various power-related parameters, further supports the superiority of the 18T-FA circuit, making it a promising candidate for future on-chip applications demanding efficient arithmetic operations.

References

[1] D. H. Roberts, “Silicon integrated circuits: A personal view of the first 25 years,” Electronics and Power, vol. 30, pp. 282–284, April 1984.
[2] J. S. Kilby, “The integrated circuit’s early history,” Proceedings of the IEEE, vol. 88, pp. 109–111, Jan 2000.
[3] N. Srivastava and K. Banerjee, “Performance analysis of carbon nanotube interconnects for vlsi applications,” in IEEE/ACM International Conference on Computer-Aided Design, pp. 383–390, Nov 2005.
[4] S. Kang and Y. Leblebici, CMOS Digital Integrated Circuits Analysis & Design. New York, NY, USA: McGraw-Hill, Inc., 3 ed., 2003.
[5] E. Mollick, “Establishing moore’s law,” IEEE Annals of the History of Computing, vol. 28, pp. 62–75, July 2006.
[6] M. Horowitz, “Scaling, power, and the future of cmos technology,” in Device Research Conference, pp. 7–8, June 2008.
[7] F. Schwierz, J. Pezoldt, and R. Granzner, “Two-dimensional materials and their prospects in transistor electronics,” Nanoscale, vol. 7, pp. 8261–8283, 2015.
[8] A. B. Kahng, “The itrs design technology and system drivers roadmap: Process and status,” in Proceedings of the 50th Annual Design Automation Conference, DAC ’13, (New York, USA), pp. 34:1–34:6, ACM, 2013.
[9] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer cmos circuits,” Proceedings of the IEEE, vol. 91, pp. 305–327, Feb 2003.
[10] C. Durkan, Current at the Nanoscale. World Scientific, 2nd ed., 2013.
[11] K. Saraswat, H. Cho, P. Kapur, and K. H. Koo, “Performance comparison between copper, carbon nanotube, and optical interconnects,” in IEEE International Symposium on Circuits and Systems, pp. 2781–2784, May 2008.
[12] A. Naeemi, R. Sarvari, and J. D. Meindl, “Performance comparison between carbon nanotube and copper interconnects for gigascale integration (gsi),” IEEE Electron Device Letters, vol. 26, pp. 84–86, Feb 2005.
[13] P. Avouris, A. Afzali, J. Appenzeller, J. Chen, M. Freitag, C. Klinke, Y. Lin, and J. C. Tsang, “Carbon nanotube electronics and optoelectronics,” in IEDM Technical Digest. IEEE International Electron Devices Meeting., pp. 525–529, Dec 2004.
[14] D. Hisamoto, Wen-Chin Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T. J. King, J. Bokor, and C. Hu, “A folded-channel mosfet for deep-sub-tenth micron era,” in International Electron Devices Meeting, pp. 1032–1034, Dec 1998.
[15] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau, “Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering,” in Symposium on VLSI Technology, Digest of Technical Papers., pp. 50–51, June 2006.
[16] D. S. Holmes and E. P. De Benedictis, “Superconductor electronics and the international roadmap for devices and systems,” in 16th International Superconductive Electronics Conference (ISEC), pp. 1–3, June 2017.
[17] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, “High performance silicon nanowire field effect transistors,” Nano Letters, vol. 3, no. 2, pp. 149–152, 2003.

[18] T. Ashley, A. R. Barnes, L. Buckle, S. Datta, A. B. Dean, M. T. Emery, M. Fearn, D. G. Hayes, K. P. Hilton, R. Jefferies, T. Martin, K. J. Nash, T. J. Phillips, W. A. Tang, P. J. Wilding, and R. Chau, "Novel insb-based quantum well transistors for ultra-high speed, low power logic applications," in Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology, vol. 3, pp. 2253–2256, Oct 2004.
[19] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, "85nm gate length enhancement and depletion mode insb quantum well transistors for ultra high speed and very low power digital logic applications," in IEEE InternationalElectron Devices Meeting, pp. 763–766, Dec 2005.
[20] T. Ashley, A. B. Dean, C. T. Elliott, R. Jefferies, F. Khaleque, and T. J. Phillips, "High-speed, low-power insb transistors," in International Electron Devices Meeting, pp. 751–754, Dec 1997.
[21] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Roomtemperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," Phys. Rev. Lett., vol. 100, p. 206803, May 2008.
[22] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene fieldeffect device," IEEE Electron Device Letters, vol. 28, pp. 282–284, April 2007.
[23] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene fieldeffect transistor with al2o3 dielectric," Applied Physics Letters, vol. 94, no. 6, p. 062107, 2009.
[24] A. Javey, J. Guo, Q. Wang, M. S. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," Nature, vol. 424, pp. 654–657, 2003.
[25] J. Deng, N. Patil, K. Ryu, A. Badmaev, C. Zhou, S. Mitra, and H. P. Wong,M "Carbon nanotube transistor circuits: Circuit-level performance benchmarking and design options for living with imperfections," in IEEE International Solid-State Circuits Conference, pp. 70–588, Feb 2007.