Semiconductor Optoelectronics
ISSN: 1001-5868

60NW POWER, HIGH-SPEED PSEUDO-RANDOM CLOCK GENERATOR WITH 4-BIT LSFR BASED ON HIGH PERFORMANCE XOR AND ENHANCED DUAL EDGE TRIGGERED D FLIP FLOP FOR AIC

R.Rajalakshmi [a, 1], R.Rajalakshmi [b], Dr.M.Janaki Rani [c], Dr.M.Anand [d]
[a] Research Scholar, Dept of ECE, Dr.M.G.R Educational & Research Institute University, Maduravoyal,Chennai,India.
[b] Assistant Professor Grade-1, Dept of ECE, Panimalar engineering college,Chennai.
[c, d] Professor, Dept of ECE, Dr.M.G.R Educational &Research Institute University, Maduravoyal,Chennai,India.
Corresponding author: 1* R Rajalakshmi; email id: mailtorajalakshmi2020@gmail.com

Abstract— In the proposed work, the effects on the LFSR (linear feedback shift register) were investigated, along with XOR and a signal feed-through-based dual edge-triggered D flip flop with low power consumption. Consider the power dissipation and critical path delay while evaluating the performance parameter. lowering the transistor count in the stack, and when compared to other flip-flops, the operational speed increases as the number of charge paths increases. We propose a new technique for implementing low-energy dual-edge triggered flip-flops in this paper. The new technique employs a clock branch-sharing scheme to reduce the number of clocked transistors in the design. The newly proposed design also employs conditional discharge and split-path techniques to further reduce switching activity and short-circuit currents, respectively. The simulations of LSFR, XOR, and D-FF are done using Tanner EDA Tool V16.1 with CMOS 180nm, 90nm, and 45nm technologies.
Keywords— LSFR, PRNG, MCML, DCML, DETFF, XOR, Analog-to Information Converter (AIC),

I. INTRODUCTION

WITH the increasing use of ambulatory monitoring system, not only continuous signal collection and low-power consumption, but also smartness with robust operation under the patients' daily routine is required. The target is emerging to enable configurability for different applications, ranging from simple heart rate calculation towards more complex medical diagnostics under ambulatory conditions, with extreme low power consumption and high accuracy Fig. 1.

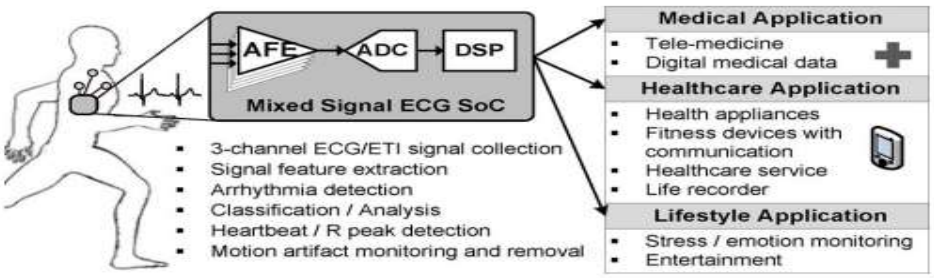

Fig 1. Mixed-signal ECG SoC and typical applications.

In order to address this challenge, local data processing with advanced functionalities is required, such as motion artifact reduction and accurate feature detection. However, these

additional functionalities lead to increased computation complexity [1]. Previous solutions using a general-purpose processor have limited functionality, limited programmability, or cannot achieve very low power consumption. Though, the processors, are implemented to optimize the biomedical signal processing, they include only the digital processor, so need the external sensor module for biopotential signal acquisition. It increases the system power consumption due to the data transmission between the modules, as well as the system form-factor. This drives the integration of the proposed mixed signal system-on-chip (SoC) combining a low-power analog-front-end (AFE) with a fully optimized and configurable digital signal processor back-end (DBE). This paper presents a biopotential acquisition unit with analog-to-information converter for medical wearable health monitoring applications. The bio signal amplifier defines the quality of the acquired biopotential signals. At the heart of the system is an Analog to Information Converter (AIC) to enables the random under sampling operation [1], [2]. AIC is used to digitize the output of the bio signal amplifier fig. 2. The sampling rate of traditional analog-to-digital conversion (ADC) architectures needs to be at least twice the signal bandwidth to achieve alias free sampling [1]-[2]. The increasing demand for systems with both higher bandwidth and lower power consumption motivates the research of innovative ADCs, especially when sampling rates reach several GHz.

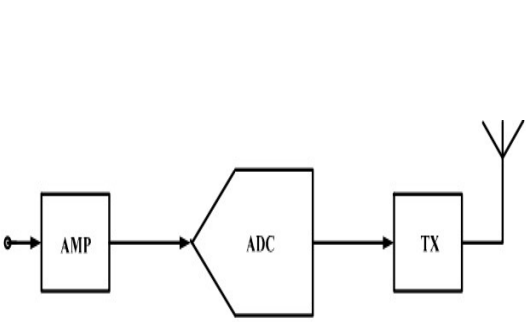

Fig. 2(a) Biopotential acquisition system

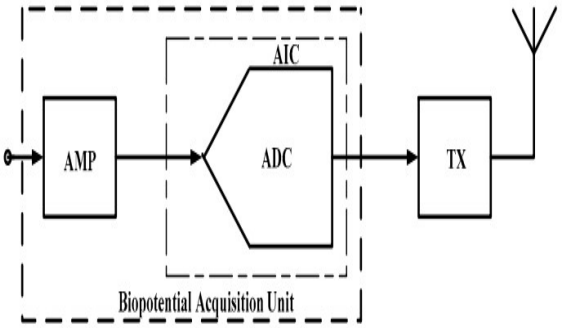

Fig. 2(b) Compressed sensing based biopotential acquisition system

Significant development has been made in the field of Biomedical Electronics since past few years. Equipment Design for Biomedical Data Acquisition and Analysis has gained the worthy attention of Researchers [3]–[5]. Biopotential acquisition unit plays very important role as a front-end design for such equipment. The design contains Pre-Amplifier, Bio signal Amplifier, filters and Analog to digital converter (ADC) which needs to be integrated on single chip to provide SoC (System-on-Chip) solution.Most hardware development of fully integrated, biopotential acquisition systems to-date, is still in the proof-of-concept stage. To be ready for practical use, the trade-offs between performance, power consumption, device size, robustness and compatibility need to be carefully taken into account [6].

The next part provides a thorough explanation of the proposed biopotential acquisition unit related works are shown in Section 2. Section 3 describes the DAC unit, while Sections 4 and 5 explain a P-N sequence generator using LFSR and enhanced dual edge triggered D FF. Sections 6 deals the simulation findings and performance overview. Finally, Section 7 discusses this work's conclusions.

I. BIOPOTENTIAL ACQUISITION UNIT:

Reliable, long-term biopotential signals monitoring is one of the crucial part in biomedical research and clinical treatment. This has a few challenges of its own like biomedical signal contains very small amplitude in the range of hundreds of micro to some milli volts and frequency variations around tens of hertz with significant interference act like common mode

voltage [2]. To sense such type of low amplitude and frequency signal, the amplifier should have a good gain along with high Common Mode Rejection Ratio (CMRR). The design optimizations of a fully integrated biopotential system with on-chip data compression is thus highly desired. An ADC is an integral part of any biopotential acquisition unit. Flash ADCs are used for high-frequency applications where dissipated power is very high. The pipeline, folding and interpolating ADCs are used when higher resolution than that of flash ADC is required at the cost of lower speed. Sigma-Delta is preferred for the highest resolution converters operating at lower speeds. Finally, successive approximation register (SAR) converters exhibit the lowest dissipated power with moderate resolution at relatively lower data rates. hence SAR ADC is required to design an ultra-low power acquisition unit [7].

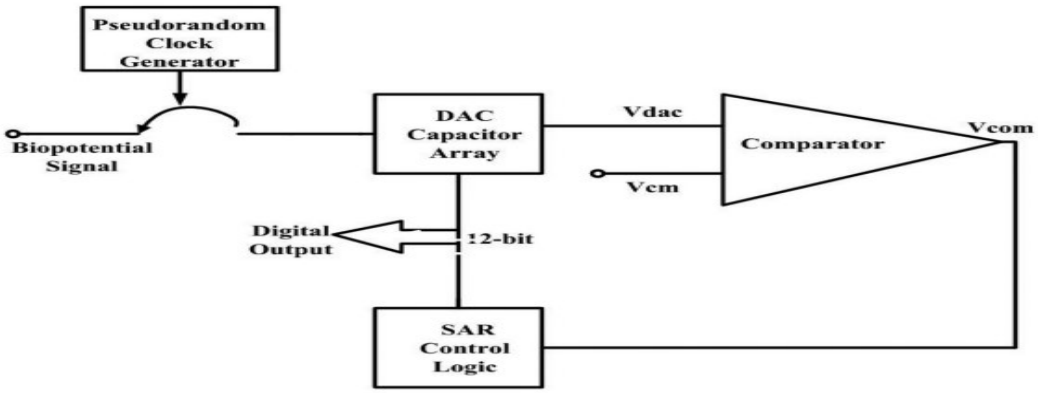

Fig. 3. Analog-to-Information Converter (AIC)

Here, the Analog-to-Information Converter (AIC) consists of a SAR ADC with a random clock edge generator. In this AIC design, charge redistribution Digital-to-Analog Converter (DAC) is used for area efficiency. Compared to conventional DAC architecture, a charge redistribution DAC array internally performs the sample and hold operation. Therefore, the sample and hold block is not needed in this implementation. In order to reduce the power consumed by the DAC, we have employed smaller size capacitors. To reduce the power consumption further, a dynamic latch type comparator is incorporated in the design [8].

A conventional biopotential acquisition system is shown in Fig. 2(a) and the block diagram for compressed based acquisition system is shown in Fig. 2(b). The power consumption (Psys) of the system shown in Fig. 2 (a) is given by,

$$\boldsymbol{P_{total} = P_{Bio\ Amp} + P_{ADC} + P_{TX}} \quad \text{_____(1)}$$

where P_{total} is the total power consumption of the system, $P_{Bio\ Amp}$ is the power consumption of Bio signal amplifier, P_{ADC} is the power consumption of ADC, P_{TX} is the power consumption of Transmitter.

$$\boldsymbol{P_{TX} = J\ F_S\ R}$$

where F_S is ADC sampling frequency, R is the number of bits per sample and J is the net transmission power per bit. JF_SR gives transmitter power consumption [9], [10]. The power consumption (Ptotal_CS) for compressed sensing-based system is,

$$\boldsymbol{P_{total\_CS} = P_{Bio\ Amp} + P_{AIC} + \frac{M}{N} P_{TX}} \quad \text{_____(2)}$$

Where P_{total_CS} is total power consumption for compressed sensing-based system, $P_{Bio\ Amp}$ is the power consumption of Bio signal amplifier, Here the Bio signal amplifier power consumption is same for both the cases. For compressed sensing system, a pseudorandom clock generator (PN) is used to generate random clock sequence and that adds to total system power and P_{AIC} includes that overhead. In addition to this, the power required to transmit the number of data bits (JF_SR in (1)) has been reduced by a factor of M/N in equation (2) compressed sensing-based system approach.

II. DAC UNIT:

A series of three processes called "sample mode," "hold mode," and "redistribution mode" are used to complete the DAC conversion. In the sample mode, the input voltage (V_{CM}) is applied to the top plates of all capacitors and the input voltage (V_{IN}) to the bottom plates. As a result, the capacitor array samples the input voltage. Switches link the bottom plates to the ground while in hold mode. As a result, the capacitor array stores a charge equal to V_{IN} plus V_{CM}. The status of switches is determined by digital code at the start of the redistribution mode, and this mode is where the actual conversion is done. D_{11} is high at the start of conversion, therefore V_{REF} is linked to the MSB capacitor. At this stage, the equation below provides the DAC's output voltage.

$$V_{DAC} = - V_{IN} + V_{CM} + V_{REF}/ 2 \quad \_\_\_\_\_ (3)$$

At the conclusion of one conversion period, the output voltage of the charge redistribution DAC is given by eqn (3). This process continues up to the next sample mode operation. Several parameters, such as thermal noise, capacitor matching, the magnitude of the parasitic capacitances, or technological design guidelines, have an impact on the minimum value of the unit capacitor . The value should be as low as feasible to reduce power consumption. We chose a unit capacitance value of 20 fF in consideration of the procedure and resolution described in [7]. Based on the unit capacitance, the values of the other capacitors in the capacitor array are established. We effectively replace the Nyquist sampling SAR ADC with a SAR ADC with pseudorandom clock generator to provide random under samples.

$$V_{DAC} = - V_{IN} + V_{CM} + D_{11} V_{REF} /2^0 + D_{10} V_{REF}/ 2^1 + \cdots + D_1 V_{REF}/ 2^{11} + D_0 V_{REF} /2^{12} \quad (4)$$

III. A P-N SEQUENCE GENERATOR USING LFSR WITH ENHANCED DUAL EDGE TRIGGERED D FF:

This paper represents the design and implementation of a low power 4-bit LFSR using enhanced dual edge triggered flip flop (EDEDFF). A linear feedback shift register (LFSR) is assembled by N number of flip flops connected in series and a combinational logic generally XOR gate. An LFSR can generate random number sequence which acts as cipher in cryptography. In this paper a novel circuit of random sequence generator using enhanced set /reset flip flop has been proposed. Data has been generated on every transition of flip flop instead of single edge [11]. A EDEDFF-LFSR can generate random number require with a smaller number of clock cycle, it minimizes the number of flip flop result in power saving. The problem of getting high output with low power consumption is addressed by electronics circuit like LFSR [5].

To increase the battery life of different component as well as to reduce noise cooling and heat dissipation, low power consumption is needed. Random number are very important for various bio medical applications for wide range in science and engineering that involve statistical random input, random number are needed . A generator of Pseudo-random number is device that generates a sequence of symbol of number with no well-defined pattern. True random number generator [TRNG] and pseudorandom generator [PRNG] are two way to generate random sequences. TRNG is a random generator which measure some physical method that is calculated to be random and then pay off for potential biases in the measuring process, whereas PRNG uses mathematical algorithm which produce random number sequence that are entirely decided by a primary value called a seed, while LFSR provide very fast random sequence generator. There are two types of LFSR such as

1. Galois implementation
2. Fibonacci implementation

Galois implementation: The Galois implementation is also known as m-type LFSR in which the flowing of data is done from left to right and feedback is done from the right side to left

side and polynomial order of shift register increments from left to right starting from X_0.

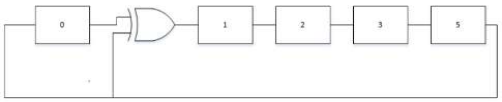

Fig. 4. Galois LSFR implementation

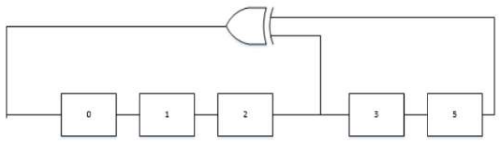

Fig. 5. Fibonacci implementation

Here in Galois Implementation output of one shift register is going as an input of next shift register at every positive edge of the clock and at the taps, where output of shift register is going as an input to the Ex-Or gate with the output bit before going in to the input of next shift register. PBRS equation generated by Galois implementation is $F(X) = X^5 + X^1 + 1$.

Fibonacci implementation:

The Fibonacci implementation is most commonly used type of LFSR, it is also known as simple type or out of line LFSR. In this implementation data flowing is done from left to right and feedback path is reverse of that, right to left. The bit positions that have an impact on next input bit are called taps. The furthest right bit is called output bit and polynomial order of the shift register increments from right to left. Fig. 5. displays the block diagram of the Fibonacci implementation.

In Fibonacci implementation output of each shift register is an input to the next shift register and new bit is generated by Ex-OR ing of all taps with output bit and it goes to the input to the left most shift register. Total number of bits generated by LFSR before repeating the same sequence are $2^m - 1$, where m is number of shift registers. The equation of the sequence generated by the figure shown above is $F(X) = X^5 + X^2 + 1$. LFSR circuit has two major components- positive edge trigger D-FF Fig. 8. and minimum power XOR circuit. Realization of LFSR can be done by using internal as well as external feedback system. In external feedback system, the paths of desired FF are passing through XOR gate whereas for internal feedback system, between the pair of FF design only one XOR gate is present without considering the size of FF used. Comparing both the models, type I feedback system is much better then type II because of its higher operating frequency. So, we have focused on type I for overall circuit analysis. The polynomial used is represented in Fig. 6. as $P(x) = x4 + x3 + x1 + 1$, n=4 Where, n is the degree of polynomial that tells number of nodes in the circuit. Using same clock signal in feedback system increases the relation between FF used which thereby results in power reduction. If number of test vector is increased, switching activity between FF decreases which is another way of reducing power dissipation [12], [13].

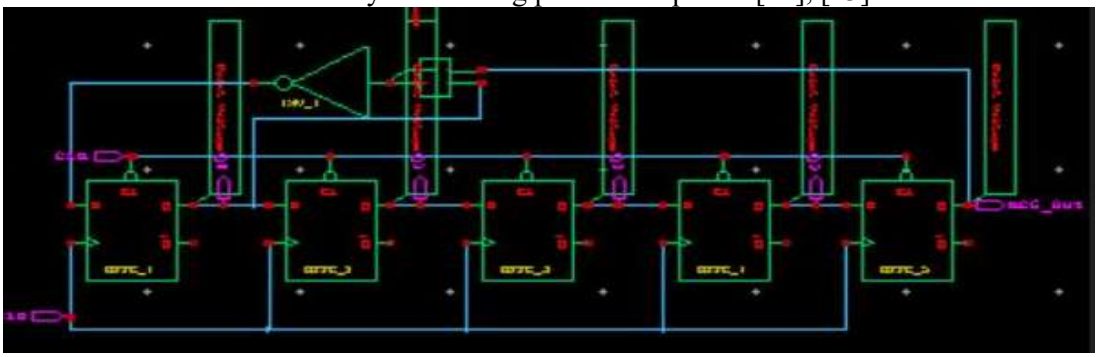

Fig. 6. 4 BIT LSFR WITH ENHANCED XOR

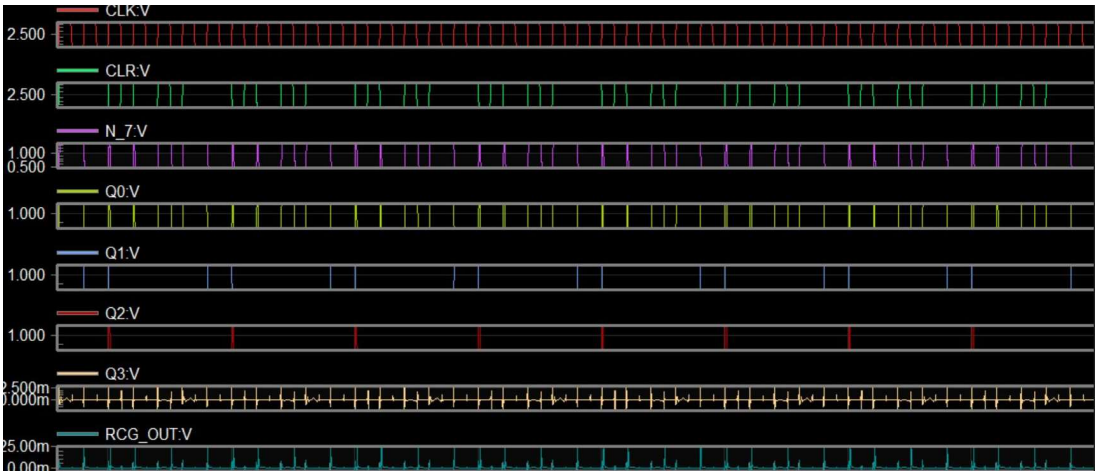

Fig. 7. 4 BIT LSFR WITH ENHANCED XOR OUTPUT

Figure 6 & 7 shows the schematic diagram and simulated outcomes of 4-bit LSFR with enhanced XOR gate technique.

IV. DETFF:

The result of D FlipFlop (DFPFP) will be same as input but with some delay. D denotes data, it stores the information given. In order to the D input, the clock signal should be active then only the correct output will be obtained. And this contains set (or) reset design with the CMOS inverter design. There are two types of DFPFP those are single edge triggered (SET) and double edge triggered (DET) SET is uncomplicated and very easy to project the performance on enhancing and reducing edges of the clock pulse. The implementation of TSPC DFPFP is with 5 transistors and it is visualized in the Fig. 8. And this design consists of 3NMOS and 2PMOS transistors [14].

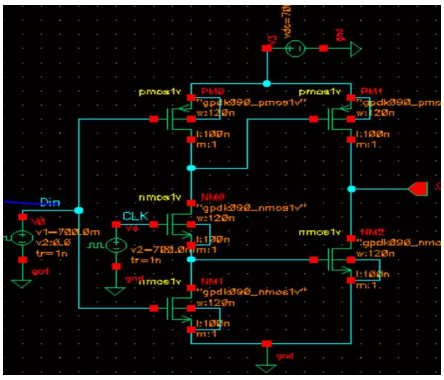

Fig. 8. TSPC DFPFP

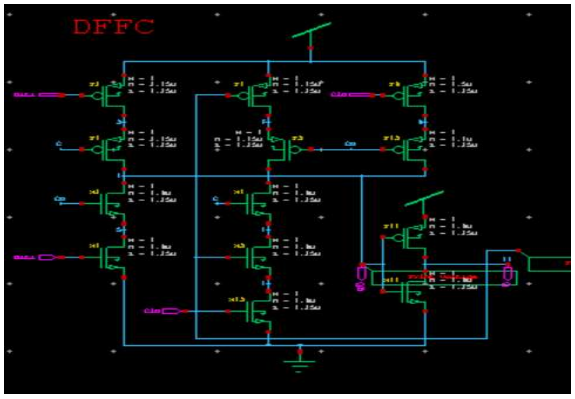

Fig. 9. Dual Edge Triggered D Flipflop

This FlipFlop is designed with miniature in nature because of a smaller number of transistors so that it reduces the power dissipation. TSPC stands for true single phase clocked logic design uses one aspect of clock Pulse and avoid skew Problems while designing and performs well in digital structure [14]. Because of this reason low power consumption is observed. When the clock pulse and input D are employed then transistors P1, N3 gets off and unused transistors P2, N1, N2 gets ON. The result gets enhanced and highlighted. If the clock pulse is high or if it is ON state and the input is given then accordingly to the clock pulse given the output is changed.

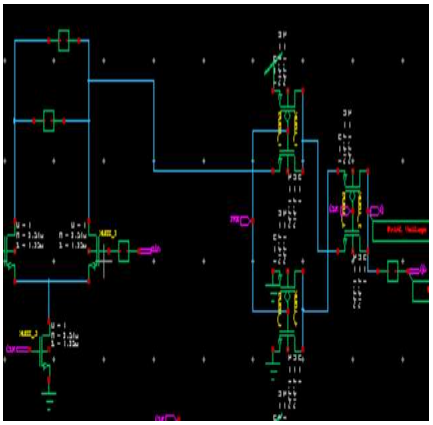

Fig. 10. ENHANCED D Flipflop

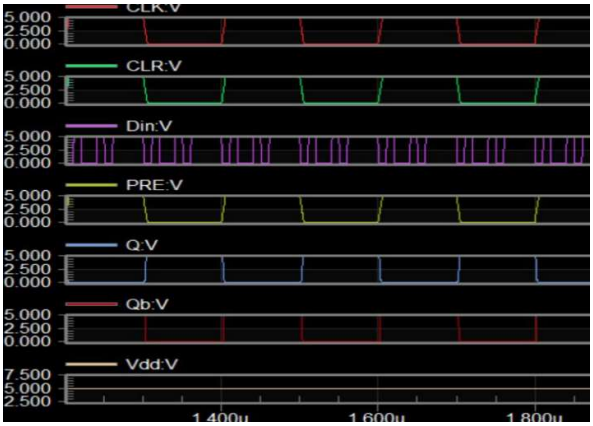

Fig. 11. Dual Edge Triggered D Flipflop Output

In enhanced DFPFP method, the power dissipation gets optimized in addition leakage current flow also gets minimized because of the connection of extra two transistors. The basic is that supply potential for the flip-flop design is substantially optimized in static mode. The power dissipation at ideal condition is directly connected to supply potential and current, such that power dissipation is shortened for same value because of enhanced supply voltage levels. This technique helps to optimized the power dissipation, in addition count of clocked transistors gets minimized [15]. Hence working speed of design increases and also the dynamic power consumption gets optimized.

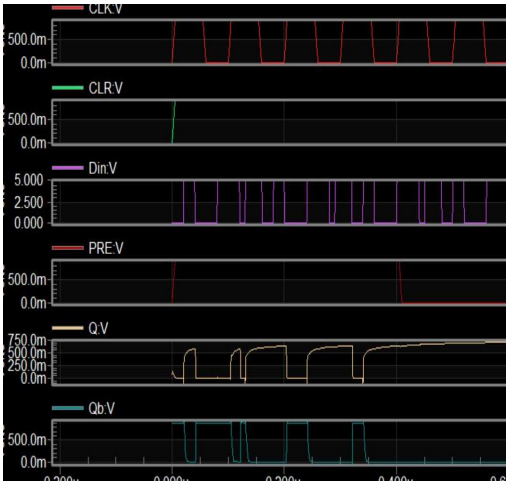

Fig. 12. Enhanced Dual Edge Triggered D Flipflop Output

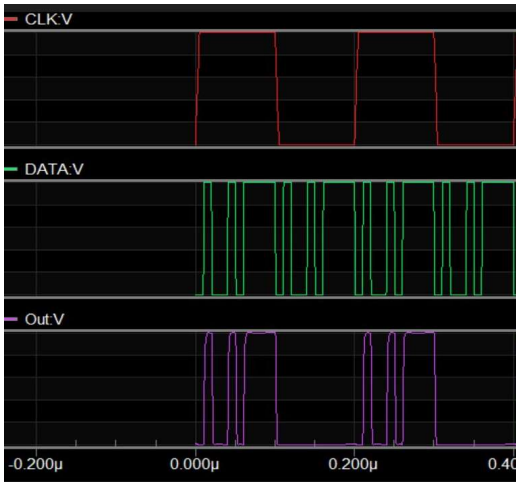

Fig. 13. TSPC DFPFP OUTPUT

V. RESULT AND DISCUSSION:

The simulated outcomes of CMOS DFPFP using tanner EDA tool using 45nm CMOS technology with supply potential of 0.9V is showed in fig. 12. By using the projected techniques, the power dissipation, propagation delay constraints get optimized. Specifically, the enhanced dual edge triggered method for CMOS DFPFP design gives better results in terms of power dissipation, leakage current and propagation delay. Mainly by optimizing the width to length ratio of transistors the three constraints optimized automatically.

Power dissipation

Pleak = Ileak.Vdd

Propagation delay = 0.69 Req x CL
CL= Load capacitance; Req= equivalent resistance

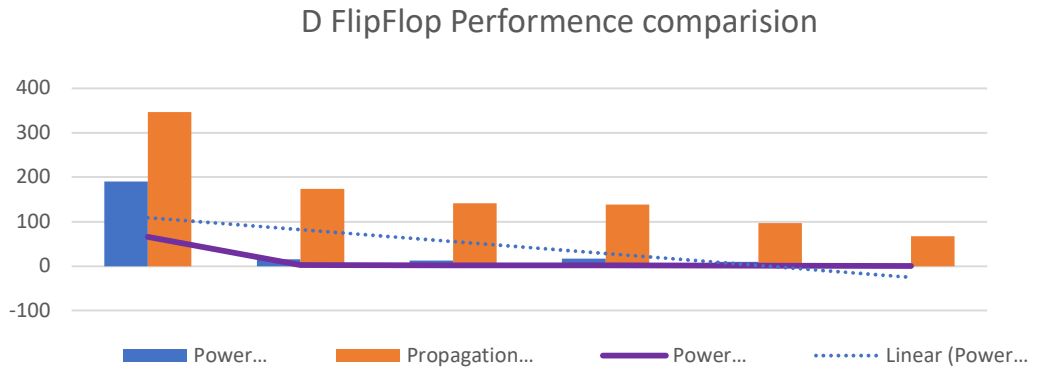

Fig. 16. D FlipFlop Performence comparision

Table 3. D FlipFlop Performence comparision

PERAMETERS	CMOS D FF	CMOS DEFF	CMOS ENHANCE DEFF	CMOS D FF	CMOS DEFF	CMOS ENHANCE DEFF
Technology Applied	90nm	90nm	90nm	45nm	45nm	45nm
Supply Voltage	1.8V	1.8V	1.8V	0.9V	0.9V	0.9V
Power Dissipation(nW)	190.84	15.54	12.87	16.58	9.86	4.48
Propagation Delay(nS)	346.8	173.6	141.3	138.6	96.7	67.8
Power delay product (10-15 J)	65.74	2.7	1.808	2.23	0.947	0.301

The 4-bit LFSR circuit using PTL logic based XOR is simulated using CMOS 90 nm technology in Tanner EDA. Below table. 1. shown the performance of the PTL logic based XOR as well as compare various XOR gate based on different technique from literature. We study and analyze the impact of various XOR circuits which is one of the major components of LFSR circuit in contribution towards low power and high performance. The performance comparison is done in terms of power dissipation and delay. As a result, the proposed XOR has minimum amount of power dissipation and delay.

Table. 1. XOR performance comparison

Logic Gate		CMOS	Literature [12]	Proposed LFSR
XOR	Power (mW	1.06	0.6	167(nW)
	Delay (us)	1.02	0.5	299(ps)

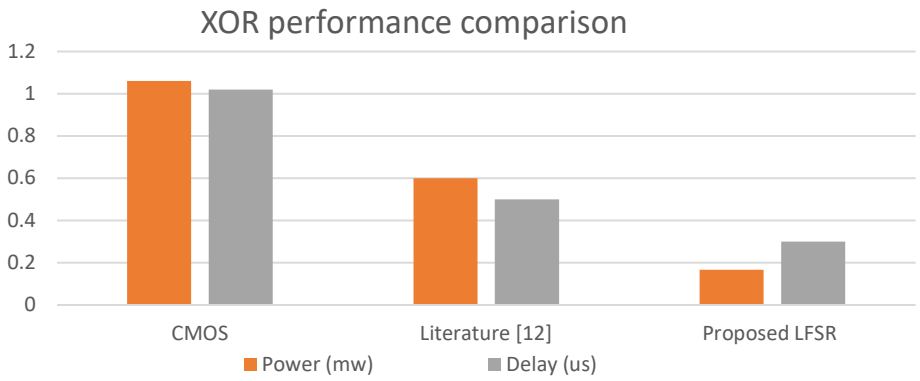

Fig. 14. XOR performance comparison

We examine MOS current mode logic, dynamic current mode logic and pass transistor logic based XOR circuit in order to find the effectiveness on LFSR circuit. In order to evaluate the performance parameters such as delay, power dissipation and chip area, Tanner EDA V16.1 tool is used. We found the PTL logic based XOR circuit has tremendous improvement in terms of power, delay and chip area and contrast to previous literature. After getting the improvement on PTL based XOR gate, we design the LFSR circuit to obtain the impact of XOR gate with various design technique. 4-bit LFSR based on XOR circuit given the high improvement in terms of power dissipation as compared to previous LFSR [15].

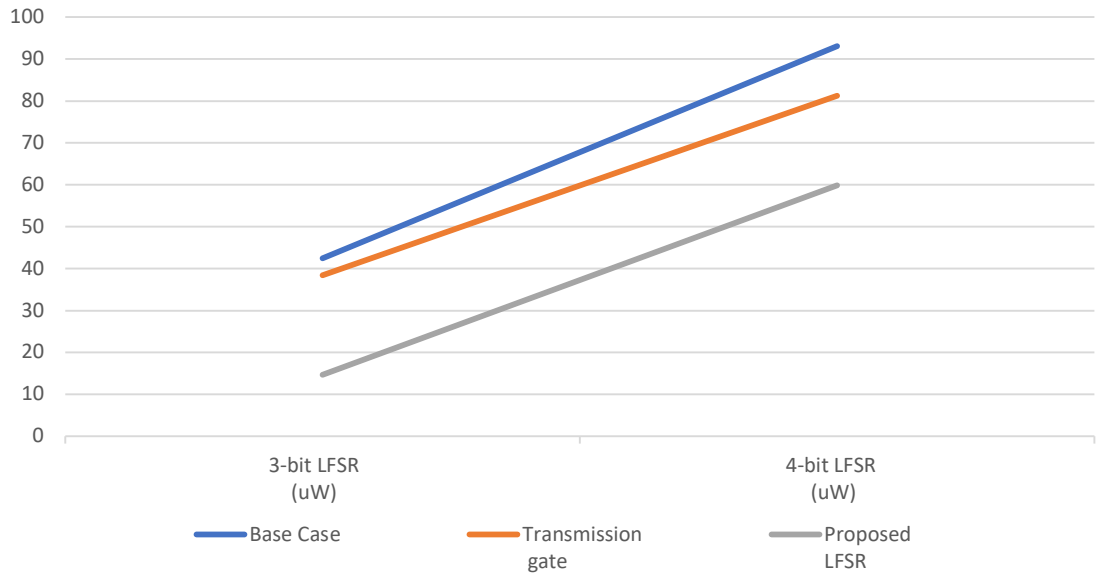

Fig. 15. LSFR performance comparison

Table. 2. LSFR performance comparison

PowerReduction Approach	3-bitLFSR (uW)	4-bitLFSR (uW)
Base Case	42.49	93.06
Transmission gate	38.39	81.21

Proposed LFSR	14.712	**59.901**

VI. CONCLUSION:

In VLSI technology, CMOS DFPFP uses less power, mostly for battery needs. The low-power CMOS DFPFP circuit was constructed using the enhanced dual edge triggered method. By using this method, the circuit was enhanced in terms of power dissipation, better backup, and supply potential. A CMOS dual edge DFPFP technique applied to the enhanced DFPFP architecture optimises power usage(4.48nW) and leakage currents to a limited extent. Less-clocked transistors in the proposed schematic design reduce dynamic power consumption as well as leakage current for the necessary circuit. In order to determine the effectiveness of the LFSR circuit, we investigate MOS current mode logic, dynamic current mode logic, and a transistor logic-based XOR circuit. Tanner EDA V16.1 tool is used to assess performance factors power dissipation, and Delay. In comparison to earlier literature, we discovered that the PTL logic-based XOR circuit has a significant improvement in terms of power, delay, and chip space. We develop the LFSR circuit to obtain the influence of the XOR gate with various design techniques after obtaining an improvement on the PTL-based XOR gate. Given the significant reduction in power consumption (59.9uW) compared to the prior LFSR, a 4-bit LFSR based on an XOR circuit was used.

REFERENCES:

[1] F. Pareschi, M. Mangia, P. Albertini, R. Rovatti, G. Setti, and G. Frattini, “An Analog-to-Information converter for Biomedical Signals based on Compressive Sensing.”

[2] W. Singh, A. Shukla, S. Deb, and A. Majumdar, “Energy efficient EEG acquisition and reconstruction for a Wireless Body Area Network,” *Integr. VLSI J.*, vol. 58, pp. 295–302, Jun. 2017, doi: 10.1016/j.vlsi.2016.08.006.

[3] R. Rajalakshmi, M. Janaki Rani, and M. Anand, *A contemporary survey on low power, high speed comparators for bio-medical applications*, vol. 38. 2021.

[4] B. Abinaya, A. P. Abirami, J. Divya, and R. Rajalakshmi, “Wireless charger for artificial pacemaker,” in *Advances in Parallel Computing*, 2021, vol. 38, pp. 527–531, doi: 10.3233/APC210096.

[5] G. Gifta *et al.*, “An Analog Front-End for a Multifunction Sensor Employing a Weak-Inversion Biasing Technique with 26 nVrms, 25 aCrms, and 19 fArms Input-Referred Noise,” *IEEE J. Solid-State Circuits*, vol. 8, no. 13, pp. 171–173, Nov. 2020, doi: 10.1109/JSSC.2016.2581812.

[6] J. M. Arunthathi *et al.*, “Ultra-low-power Circuits and Systems for Wearable and Implantable Medical Devices,” *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 1642, no. 1, p. 231, 2020, doi: 10.1109/JSEN.2016.2564942.

[7] V. Meerajahana, P. Vedhanayagi, and K. Ramasamy, “Design of Low power Successive Approximation Register ADC Using 14 bit Two-Split Capacitor DAC Array,” no. 8, pp. 270–275, 2016.

[8] J. H. Kim, J. H. Lee, and J. H. Cho, “Implementation of integrated circuit and design of SAR ADC for fully implantable hearing AIDS,” in *Technology and Health Care*, Jul. 2017, vol. 25, no. S1, pp. S83–S92, doi: 10.3233/THC-171309.

[9] I. Kim, Y. A. Bhagat, J. Homer, and R. Lobo, “Multimodal Analog Front End for

Wearable Bio-Sensors," *IEEE Sens. J.*, vol. 16, no. 24, pp. 8784–8791, 2016, doi: 10.1109/JSEN.2016.2564942.

[10] A. Kosari, J. Breiholz, N. Liu, B. H. Calhoun, and D. D. Wentzloff, "A 0.5 V 68 nW ECG monitoring analog front-end for arrhythmia diagnosis," *J. Low Power Electron. Appl.*, vol. 8, no. 3, 2018, doi: 10.3390/jlpea8030027.

[11] G. Sushma and V. Ramesh, "Low power high speed D flip flop design using improved SVL technique," *2016 Int. Conf. Recent Trends Inf. Technol. ICRTIT 2016*, 2016, doi: 10.1109/ICRTIT.2016.7569521.

[12] S. Agrawal *et al.*, "Design Low Power CMOS D-Flip Flop usingModified SVL Techniques," *Proc. 2017 Int. Conf. Intell. Comput. Control. I2C2 2017*, vol. 2015-April, no. 04, pp. 55–65, 2018, doi: 10.1109/I2C2.2017.8321854.

[13] R. Shandilya and R. K. Sharma, "High speed low power dual-edge triggered D flip-flop," *Proc. 2017 Int. Conf. Intell. Comput. Control. I2C2 2017*, vol. 2018-Janua, pp. 1–5, 2018, doi: 10.1109/I2C2.2017.8321854.

[14] P. Joshi, S. Khandelwal, and S. Akashe, "Implementation of low power flip flop design in nanometer regime," *Int. Conf. Adv. Comput. Commun. Technol. ACCT*, vol. 2015-April, pp. 252–256, 2015, doi: 10.1109/ACCT.2015.84.

[15] S. K. Singh *et al.*, "Design of Low Power and High-Speed Cmos D Flipflop using Supply Voltage Level (SVL) Methods," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 11, no. 3, pp. 2887–2904, 2020, doi: 10.1109/JSSC.2016.2625341.

R. Rajalakshmi received the B.E. degree in Electronics and Communication Engineering from the Government College of Engineering, Salem, India and the M.Tech degree in Computer Vision and Imageprocessing from Amrita School of Engineering, Coimbatore, India. She is now pursing part-time research in Efficient Analog front-end Design & Power Approaches for Wearable Medical Devices using VLSI Techniques at the Dr.M.G.R Educational & Research Institute, Deemed University, Maduravoyal, Chennai, India. She has been working as a faculty in Electronics and Communication Engineering at Panimalar Engineering College, Chennai, from 2009 onwards. She has published book chapters in Scopus related to her research. Her research interests include biosignal processing, compression, and low-power analog circuits for biomedical applications.