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HIGH PERFORMANCE VOLTAGE LEVEL SHIFTER BASED ON CURRENT MIRROR AND CURRENT LIMITER

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Abstract: In this study, a low-power, high-speed voltage level shifter based on a current mirror with reflected output is discussed (LS). Different voltage domains are connected through interface circuits called level shifters (LSs). The level shifter in this study was constructed using powerful current mirror and current limiter circuits to eliminate short circuit pathways and reduce power consumption. With an input supply voltage of 0.3 volts, the proposed the proposed current mirror and current limiter-based level shifter is capable of reaching high voltage levels of up to 1.5 volts.
Keywords: level shifter, power, area, delay, current mirror

INTRODUCTION

IoT edge devices now practically must have a wide performance envelope. While normal processes use medium computing performance to achieve high energy economy, urgent requests require instantaneous responses from high computational performance [1]. When the circuits work with subthreshold operation, high performance of computation can be achieved, whereas circuits with near-threshold operation ensures optimized efficiency of energy with and medium performance of computation. Scaling the supply voltage is a useful technique for modifying circuit parameters.

Reduced supply voltage causes a quadratic power drop in circuits. Scaling to the sub-threshold zone is not the best option because it promises to consume relatively less power and is a poor choice due to the exponentially high sensitivity to PVT fluctuation. IoT edge devices should not employ sub-threshold operation since it cannot provide enough performance. Compared to sub-threshold region the computational performance of near-threshold design (NTD) is significantly higher.

This is due to the fact that a core's energy efficiency must constantly be adjusted to

accommodate changing performance requirements, making NTD's ability to maintain effective performance and energy efficiency over a wide voltage range vital. NTD technology is therefore optimized to IoT applications.

Level shifters (LS) are needed to shift digital signals voltage levels from the near-threshold voltage level to the normal supply voltage level in order to combine the near-threshold domain with the normal voltage domain. To reduce overhead, it ie needed to keep minimum transition energy and static power, but the LS must be swift enough to meet performance standards. Furthermore, the LS employed should be as small as possible because chip space is important for Internet of Things applications. [2].

Power, delay and area are crucial factors in very large-scale industrial (VLSI). One of the most crucial aspects that must be taken into account while designing circuits is power dissipation [4]. Present day computers are having high operating frequency which in turn increases power consumption. Modern devices can be powered down using a variety of techniques. These are: (a) dynamic logic (b) clock gating (c) gate sizing (g) and (h) multiple voltage design (h) [3,4]. The first three techniques reduce capacitance or circuit activity which reduces switching power usage linearly. As a helpful tool for reducing overall power, the fourth option involves lowering the supply voltage. Different power supply voltage levels (VDD) are used to operate the circuit are used in this technique. The fundamental concept is to provide a separate low power supply VDD (VDDL) for the transistors that involved in the critical path of the circuits, while a high-power supply VDD (VDDH) is applied to the critical route transistors [5].

While raising static current, using different supply voltages enhances the performance of dynamic power consumption. The level converters can reduce static power consumption but potentially increases area as well as dynamic power, when they are positioned between the VDDL and VDDH There have been several suggestions for optimize power consumption, performance and area overhead for the level converters (LS). A simple design that has been proposed in [6] is High to Low level shifter. In this structure there are two inverters which are coupled to a low supply voltage. Usually, the regular low- to high-voltage level shifters are categorised into two categories, where both of the LS which work around the threshold voltage [7]. When the threshold voltage is higher than input operating voltage of MOS transistors, the circuit to design Low-To-High-LS circuitry is quite complex [8]. There are several designs that have been offered as solutions to this issue. One of LSs suggested is based on the Wilson current mirror level shifter circuit. This circuit uses a voltage level shifter to avoid being slowed down by its high standby power consumption. The advantage of this LS is that it can covert extremely low input voltage levels.

This work is organised as in section 1 existing designs of level shifters are discussed and proposed designs are discussed under section II. Then in section III results of the proposed level shifters are discussed and concluded in section V.

EXISTING DESIGNS

Conventional LS Using Differential Cascade Voltage Switch (DCVS) [10]

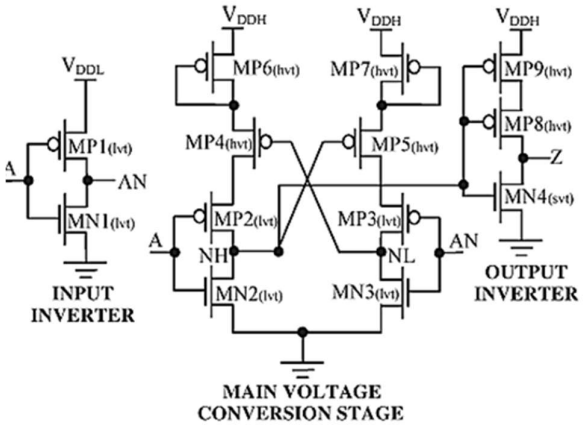

Fig.1.DCVS level shifter [9]

Fig. 1 [9] illustrates a level shifter (LS) consumes less power when the circuit shifts steady logic voltage from the near or sub-threshold to the above-threshold domain. Thanks to a unique topological modification and multi-threshold CMOS technology, the main advantage of the circuit is that it has wide voltage shifting range along with less static power and optimized overall energy consumption. The proposed design successfully shifts 180-mV input signals into 1-V output signals when simulated for 90-nm technology with operating frequencies greater than 1-MHz with consideration of process-voltage-temperature changes taking in to account. This design uses the least static energy and power possible.

Modified Wilson Current Mirror Hybrid Buffer (MWCMHB LS)

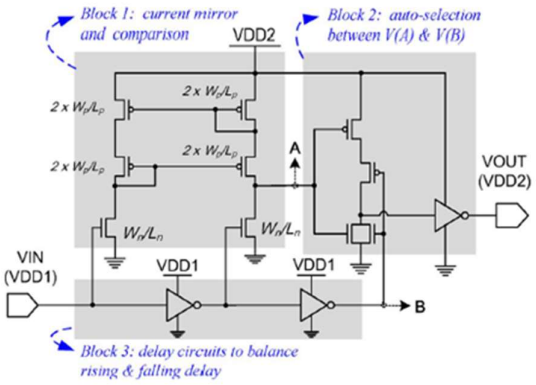

Fig.2.Modified Wilson current mirror level shifter [10]

A 50% signal duty cycle can be achieved with equal rising and falling time. If the data channel is long or for lower clock frequency this condition can be relaxed [10]. This criterion of duty cycle for Wilson Current Mirror (WCM) Level Shifter (LS) is difficult to achieve if its input and output voltage levels are near together. Since the circuit has weak Pull Up Network (PUP) it is observed that WCM LS has lengthy rising time which can be up to 100 times longer than the falling time. This severe signal skew must be corrected. In Fig. 2. Shows the Modified Wilson current mirror (MWCM) which consists of block 1 contains

Mirror circuit, block 2 auto selection circuit and block 3 delay balance circuit. At node A rising and falling delay is balanced in MWCM structure, when voltage of VDD2 is at high voltage level and VDD1 at subthreshold. This balance can be achieved without surrendering the initial

static bias which is preferred in WCM LS [6].
However, the MWCM experiences the same problem as the WCM when the VDD1 and VDD2 levels are close together: the cascode PMOS lacks sufficient driving currents, which results in an increase in latency. To decrease the growing delay and keep the duty cycle acceptable, block 3 constructs an adaptive delay path.

Pull-Up Boosted Level Shifter (PUB LS)

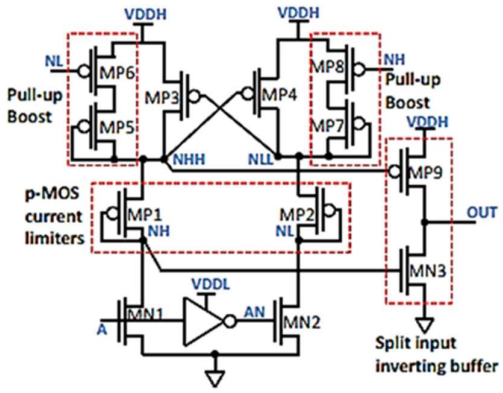

Fig.3.DCVS Pull-up boosted level shifter [11]

Lowest static power consumption can be achieved by LS architecture based on the single stage Differential Cascode Voltage Switch (DCVS) method [11] as shown in Fig.3. In order to speed switching and reduce dynamic energy consumption, it also uses self-adapting pull-up networks. An output stage with a divided input inverting buffer improves energy rapidly and efficiency even further. The voltage shifting from deep subthreshold voltage level to normal supply voltage level is achieved efficiently in the DCVS method since it employed improved self-adapting Pull Up Networks (PUNs). In order to minimize short circuit and stand-by- energy consumption the output stage contains split input inverting buffer [11].

Modified Wilson Current Mirror with Based Level Shifter (MWCMLS)

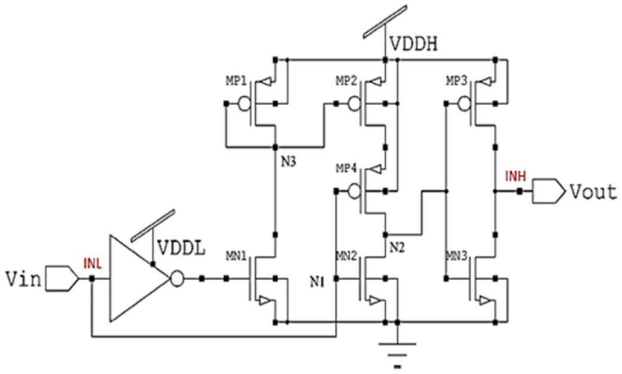

Fig.4.Modified Wilson Current Mirror with Based Level Shifter [12]

There are many supply voltages that increase static current while also raising dynamic power usage. To solve this issue the authors presented Modified Wilson Current Mirror with Based Level Shifter (MWCMLS) circuit [12] shown in Fig.4. This circuit is designed by using nine transistors and it can effectively operate up to 100 MHz of input frequency. Single threshold

voltage transistors, which are the easiest to make and use the least static power in the suggested LS, are unable to complete the entire voltage swing but are the simplest to design.

Double Current Limiter High-Performance Voltage level Shifter [13]

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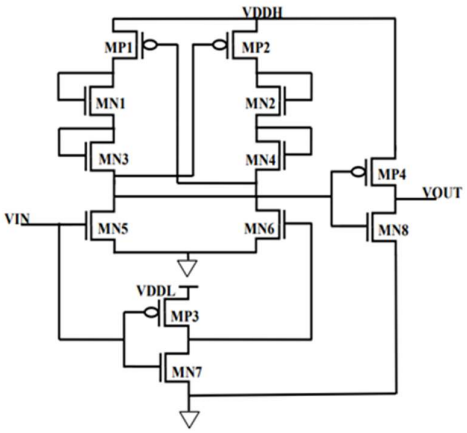

Fig.5. Double Current Limiter High-Performance Voltage level Shifter [13]

In Double Current Limiter High-Performance Voltage level Shifter as shown in Fig.5, consists of two current limiter MOS transistors MN1 and MN2 that are used in to minimize current contention [13]. Due to weak pull-down transistors, at the output full swing cannot be achieved in this method. MOS transistor MN5 turns on when the voltage input VIN changes from low to high. This will invert the MN8-MP4 inverter's output at full swing output voltage VOUT. As VIN shifts from a high to a low voltage, the short circuit current of the inverter which is connected at the output may increase. MN3-MN4 have previously added a pair of current limiters to prevent another pair from being introduced. Despite their speed, LSs based on Wilson's current mirror configuration consumes high standby power.

However, leakage current is the only technique employed by LSs based on differential cascade voltage switch topologies. However, transition time and dynamic power are also impacted by current contention between the pull-up and pull-down networks during output switching. When the input voltage level is significantly lower than the output voltage level, the issue is made worse. Sizing is a straightforward technique for balancing PDN and PUN strengths, but it produces impractical PDN sizes. To expand the voltage conversion range, a two-stage DCVS-based LS has been proposed, however, the delay is even longer. A different strategy is to use diode-connect transistors, two current generators, and self-adaptation to reduce the current contention of DCVS-based LS.

PROPOSED METHOD

The current mirror is one of the most significant analogue integrated circuits. High-performance current mirrors that can run at low voltages are required for modern VLSI systems, which are now powered by a with multiple voltages.

A low supply voltage input buffer is used for converting external input signals to internal input signals and a high supply voltage output is used to buffer for converting internal input signals to external output signals make up the voltage level shifter. The external input signal's high level is less intense than the external output signal's high level. The voltage level shifter is set

up so that the input buffer runs quickly and efficiently with little leakage. The system is still extremely intricate, and the structure includes too many devices.

With the main objective of enhancing performance in the sub threshold region in terms of power, speed and with VDDL minimum operating value, a number of sub threshold LS architectures have been proposed in the literature. The DCVS architecture is the foundation for the proposed architectures. These level shifters increase speed of the shifter by weakening the pull-up network while strengthening the pull-down network using multi-threshold CMOS techniques. Modified and controlled pull-up networks are employed to minimize power and improve speed.

The proposed level shifter circuit consists of two voltage levels one is low voltage level (VDDL) another high voltage level (VDDH), here we are able to achieve the better power consumption and delay when compared to existing voltage level shifter.

The proposed level shifter is designed by using current mirror and current limiter circuit. Current limiter circuit is used to limit the current flow and avoid the short circuit path. The simple current mirror circuit is designed by connecting the drain terminal of PMOS or NMOS to the gate terminal of the same transistor. The current in one transistor will exactly mirror that of the second, assuming that both transistors are accurately matched. It will provide the constant current.

Here input supply voltage in the range of 0.3V can able to achieve up to the high voltage level 1.5V.

The feedback transistor used by the proposed current mirror level shifter (CMLS) prevents static current from flowing during standby mode shown in Fig.6. To reduce the minimum allowable VDDL value, a modified current mirror is included in the proposed level shifter. It is suggested that in self-controlled current limiter, to minimize the power at output error detection circuit is used. To minimize the falling edge delay time, this circuit eliminates away the input inverter. The falling edge delay time is minimized by continuously charging the level-shift capacitor with a voltage equal to the voltage difference between VDDH and VDDL.

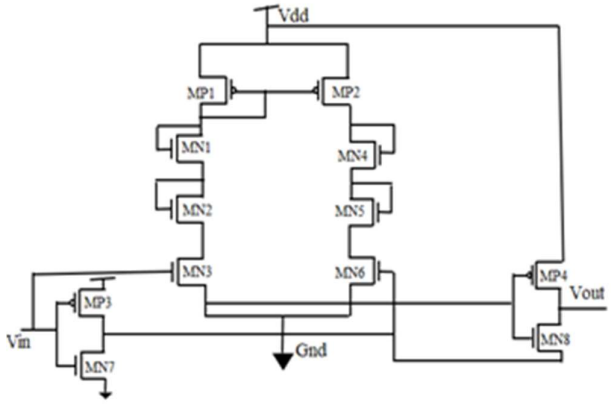

Fig.6. Schematic of the proposed LS

The parameters of the LS are compared with those of conventional LSs and Double current limiter LSs in terms of area, latency, energy, and power consumption.

The recommended High Performance Voltage Level Shifter is used as an interface circuit to lower power consumption and enhance latency. The proposed High Performance Voltage

Level Shifter will be used in IOT applications and used as a interfacing circuit.

Results and Discussion

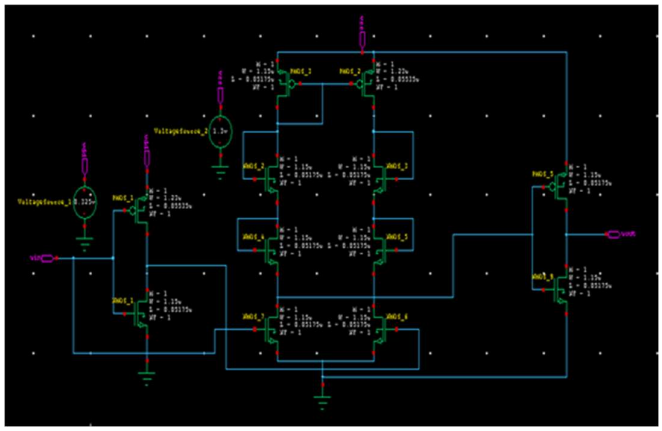

Fig.8.Implementation of Proposed Level shifter

In this work proposed level shifter is implemented in CADENCE VIRTUSO EDA tool for 45 nm technology and simulated for and observed the parameters like power delay and tabulated in Table 1. Fig.8 shows implementation of proposed level shifter in the mentioned EDA tool and it output waveforms are shown in Fig.9.

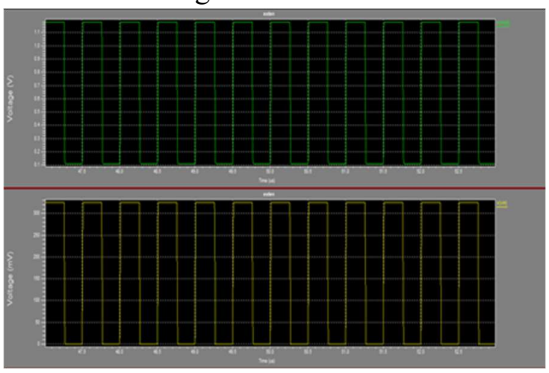

Fig .9. Simulated output of Proposed Level shifter-2

The performance parameters like area, power and Power Delay Product (PDP) for different level shifters which are existed and for proposed level shifter is tabulated in Table 1.I t is observed that proposed level shifter for the input of 0.3 V its output is shifting to 1.5 From the Table.1 it is observed that for implementing proposed level shifter it takes 12 transistor and has better performance when compared existing designs of level shifters

Table.1. Comparison between Existing & Proposed Level shifter

Design	Conversion range	Power (nw)	Delay(ns)	No pf transistors	PDP (pJ)
DCVS [9]	0.2–1.8	0.73	16.6	15	12.12
MWCMHB LS [10]	0.2–1.2	0.41	16.2	16	6.64
PUB LS [11]	0.1–1.8	0.62	31.7	14	19.65
MWCMLS [12]	0.2–1.8	0.74	19.9	9	14.73

DVSL-DCL LS [13]	0.15- 1.25	0.62	2.9	12	1.78
PROPOSED LS	0.3-1.5	0.59	0.55	12	0.33

CONCLUSION

The proposed current mirror and current limiter-based high performance voltage level shifter circuit is designed to conduct voltage level changing from 0.3V to 1.5V while utilizing 45nm CMOS technology. The results suggest that the proposed circuit switches easily and efficiently. The proposed design can be as durable as well as fulfilling all IOT needs thanks to the large conversion range.

FUTURE SCOPE

The proposed Double Current Limiter High Performance Voltage Level Shifter for IoT Applications can be improved with lower and multiple threshold devices. The proposed DFF may be implemented in complicated digital systems that integrate sequential and combinatorial logic in future study. The proposed DFF may be implemented in complicated digital systems that integrate sequential and combinatorial logic in future study. The proposed DFF may be implemented in complicated digital systems that integrate sequential and combinatorial logic in future study.

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